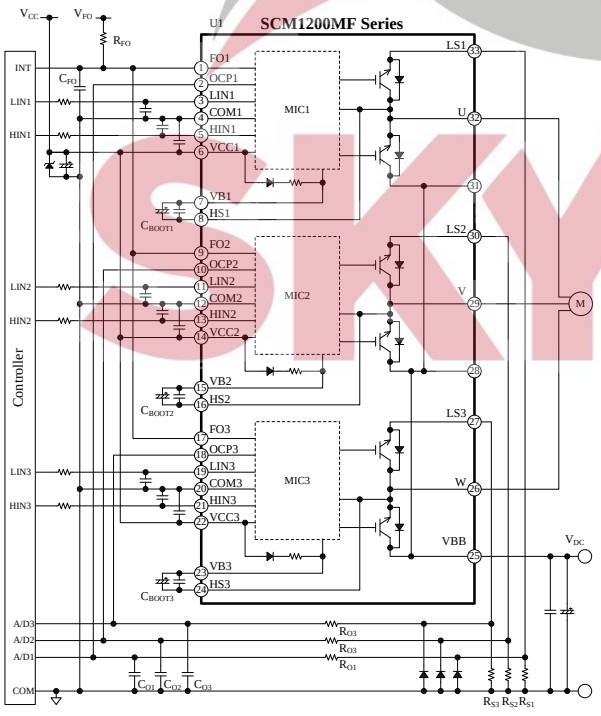
Description

The SCM1200MF series are high voltage three-phase motor driver ICs in which transistors, pre-driver ICs (MICs), and bootstrap circuits (diodes and resistors) are highly integrated. These products can run on a three-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards.

Features

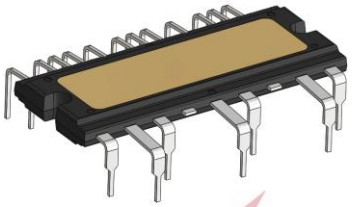
- Each half-bridge circuit consists of a pre-driver IC
- In case of malfunction, all outputs shut down via three FO pins connected together
- Built-in bootstrap diodes with current limiting resistors (22 Ω)
- CMOS compatible input (3.3 to 5 V)
- Pb free
- Isolation voltage: 2500 V for 1 min, UL recognized component (File No.: E118037)
- Fault signal output at protection activation
- Protections include:
  Undervoltage Lockout for power supply
  High-side (UVLO_VB): Auto-restart
  Low-side (UVLO_VCC): Auto-restart
  Overcurrent Protection (OCP): Auto-restart
  Simultaneous On-state Prevention: Auto-restart
  Thermal Shutdown (TSD): Auto-restart

Typical Application Diagram



Package

SCM (pin pitch: 1.27 mm, mold dimensions: 47 × 19 × 4.4 mm)



Not to scale

SCM1200MF Series

- IGBT+FRD (600 V)

I_O (A)	Feature	Part Number
10 A	Low noise	SCM1261MF*
15 A	Low noise	SCM1242MF
		SCM1263MF*
	Low switching dissipation	SCM1243MF
20 A	Low noise	SCM1265MF*
	Low switching dissipation	SCM1245MF
30 A	Low noise	SCM1256MF
	Low switching dissipation	SCM1246MF

* Uses a shorter blanking time for OCP activation.

Applications

For motor drives such as:

- Refrigerator compressor motor
- Air conditioner compressor motor
- Washing machine main motor
- Fan motor
- Pump motor

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1. Absolute Maximum Ratings

- Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).
- Unless specifically noted, T_A = 25°C.

Characteristics	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB – LS1 VBB – LS2 VBB – LS3	450	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB – LS1 VBB – LS2 VBB – LS3	500	V	
IGBT Breakdown Voltage	V_{CES}	V_{CC} = 15 V, I_C = 1 mA, V_{IN} = 0 V	600	V	
Logic Supply Voltage	V_{CC}	VCC1– COM1 VCC2– COM2 VCC3– COM3	20	V	
	V_{BS}	VB1 – HS1(U) VB2– HS2(V) VB3 – HS3(W)	20		
Output Current (DC)[1]	I_O	T_C = 25 °C	10	A	SCM1261MF
			15		SCM1242MF/63MF/43MF
			20		SCM1265MF/45MF
			30		SCM1256MF/46MF
Output Current (Pulse)	I_{OP}	T_C = 25 °C, $P_W \leq$ 1ms	20	A	SCM1261MF
			30		SCM1242MF/63MF/ 43MF/65MF/45MF
			45		SCM1256MF/46MF
Input Voltage	V_{IN}	HIN1, LIN1– COM1 HIN2, LIN2– COM2 HIN3, LIN3– COM3	−0.5 to 7	V	
FO Pin Voltage	V_{FO}	FO1– COM1 FO2– COM2 FO3– COM3	−0.5 to 7	V	
OCP Pin Voltage	V_{OCP}	OCP1– COM1 OCP2– COM2 OCP3– COM3	−10 to 5	V	
Operating Case Temperature[2]	$T_{C(OP)}$		−30 to 125	°C	
Junction Temperature[3]	T_j		150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	
Isolation Voltage[4]	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V	

[1] Should be derated depending on an actual case temperature. See Section 15.4.
[2] Refers to a case temperature measured during IC operation.
[3] Refers to the junction temperature of each chip including its built-in controller ICs (MICs), transistors, and freewheeling diodes.
[4] Refers to voltage conditions to be applied between the case and all pins. All pins have to be shorted.

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2. Recommended Operating Conditions

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	COM1 = COM2 = COM3 VBB – COM	–	300	400	V	
Logic Supply Voltage	V_{CC}	VCC1– COM1 VCC2– COM2 VCC3– COM3	13.5	–	16.5	V	
	V_{BS}	VB1 – HS1(U) VB2– HS2(V) VB3 – HS3(W)	13.5	–	16.5	V	
Input Voltage (HIN, LIN, FO)	V_{IN}		0	–	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	–	–	µs	
	$t_{IN(MIN)OFF}$		0.5	–	–	µs	
Dead Time of Input Signal	t_{DEAD}		1.0	–	–	µs	SCM1243MF/ 45MF/46MF
			1.5	–	–		SCM1242MF/ 56MF/61MF/65MF
FO Pin Pull-up Resistor	R_{FO}		1	–	22	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	–	5.5	V	
FO Pin Capacitor for Noise Reduction	C_{FO}		0.001	–	0.01	µF	
Bootstrap Capacitor	C_{BOOT}		10	–	220	µF	
Shunt Resistor	R_S	$I_P \leq 45$ A	12	–	–	mΩ	SCM1256MF/46MF
		$I_P \leq 30$ A	18	–	–		SCM1242MF/43MF/ 63MF/65MF/45MF
		$I_P \leq 20$ A	27	–	–		SCM1261MF
RC Filter Resistor	R_O		–	–	100	Ω	
RC Filter Capacitor	C_O		1000	–	2200	pF	SCM124xMF SCM125xMF
			1000	–	10000		SCM126xMF
PWM Carrier Frequency	f_c		–	–	20	kHz	
Case Temperature in Operation	$T_{C(OP)}$		–	–	100	°C	

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3. Electrical Characteristics

- Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).
- Unless specifically noted, T_A = 25°C, V_{CC} = 15 V.

3.1. Characteristics of Control Parts

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC1– COM1 VCC2– COM2 VCC3– COM3	10.5	11.5	12.5	V	
	$V_{BS(ON)}$	VB1 – HS1(U) VB2– HS2(V) VB3 – HS3(W)	10.5	11.5	12.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC1– COM1 VCC2– COM2 VCC3– COM3	10.0	11.0	12.0	V	
	$V_{BS(OFF)}$	VB1 – HS1(U) VB2– HS2(V) VB3 – HS3(W)	10.0	11.0	12.0	V	
Logic Supply Current	I_{CC}	VCC1 = VCC2 = VCC3, COM1 = COM2 = COM3 VCC pin current in 3 phases operating	–	3	–	mA	
	I_{BS}	VB – HS = 15 V, HIN = 5 V, VB pin current in single phase operation	–	140	–	μA	
Input Signal							
High Level Input Signal Threshold Voltage (HIN, LIN, FO)	V_{IH}		1.5	2.0	2.5	V	
Low Level Input Signal Threshold Voltage (HIN, LIN, FO)	V_{IL}		1.0	1.5	2.0	V	
Input Current at High Level (HIN, LIN)	I_{IH}	V_{IN} = 5 V	–	230	500	μA	
Input Current at Low Level (HIN, LIN)	I_{IL}	V_{IN} = 0 V	–	–	2	μA	
Fault Signal Output							
FO Pin Voltage in Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	–	–	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	–	–	V	
Protection							
Overcurrent Protection Threshold Voltage	V_{TRIP}		0.46	0.50	0.54	V	
Overcurrent Protection Hold Time	t_P		20	26	–	μs	
Overcurrent Protection Blanking Time	t_{BK}	V_{TRIP} = 1 V	–	1.65	–	μs	SCM124xMF SCM125xMF
			–	0.54	–		SCM126xMF
Thermal Shutdown Operating Temperature*	T_{DH}		135	150	–	°C	
Thermal Shutdown Releasing Temperature*	T_{DL}		105	120	–	°C	

* Refers to the junction temperature of the built-in controller ICs (MICs).

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3.2. Bootstrap Diode Characteristics

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	–	–	10	μA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	–	1.1	1.3	V	
Bootstrap Diode Series Resistor	R_{BOOT}		17.6	22.0	26.4	Ω	

3.3. Thermal Resistance Characteristics

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[1]	$R_{(j-c)Q}$[2]	1 element operation (IGBT)	–	–	3.7	°C/W	SCM1261MF
			–	–	3		SCM12/42MF /63MF/43MF/65MF /45MF/56MF/46MF
	$R_{(j-c)F}$[3]	1 element operation (Freewheeling diode)	–	–	4.5	°C/W	SCM1261MF
			–	–	4		SCM12/42MF /63MF/43MF/65MF /45MF/56MF/46MF

[1] Refers to a case temperature at the measurement point described in Figure 3-1, below.
[2] Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.1.
[3] Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

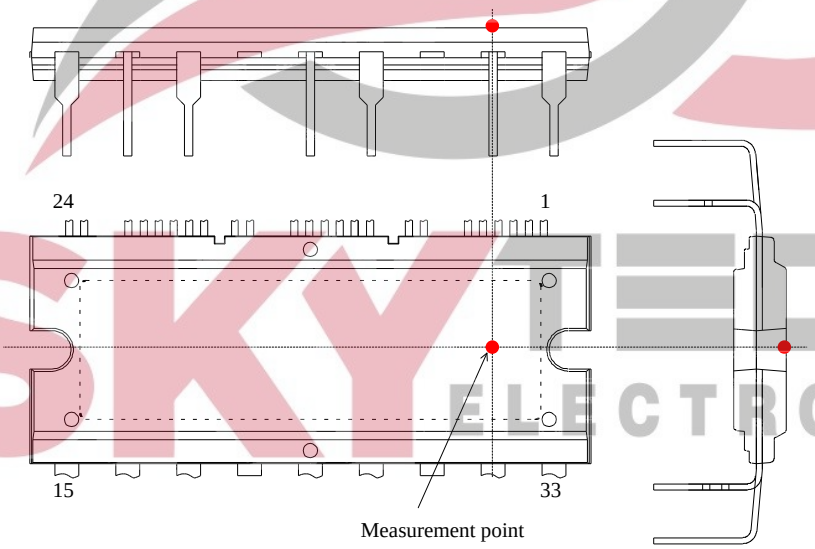

Figure 3-1. Case temperature measurement point

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3.4. Transistor Characteristics

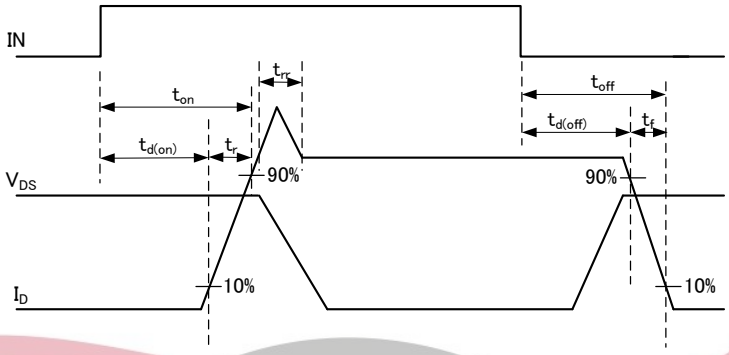

Figure 3-2. Switching time definition

3.4.1. SCM1261MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10 A, V_{IN} = 5 V	–	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 10 A, V_{IN} = 0 V	–	1.7	2.2	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 10 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	85	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	700	–	ns
Rise Time	t_r		–	100	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1070	–	ns
Fall Time	t_f		–	90	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 10 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	105	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	710	–	ns
Rise Time	t_r		–	120	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1010	–	ns
Fall Time	t_f		–	95	–	ns

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3.4.2. SCM1242MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 15 A,V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	80	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	700	–	ns
Rise Time	t_r		–	100	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1300	–	ns
Fall Time	t_f		–	90	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	90	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	700	–	ns
Rise Time	t_r		–	130	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1230	–	ns
Fall Time	t_f		–	90	–	ns

3.4.3. SCM1263MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 15 A,V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	80	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	700	–	ns
Rise Time	t_r		–	100	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1300	–	ns
Fall Time	t_f		–	90	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	90	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	700	–	ns
Rise Time	t_r		–	130	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1230	–	ns
Fall Time	t_f		–	90	–	ns

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3.4.4. SCM1243MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 15 A, V_{IN} = 5 V	—	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 15 A,V_{IN} = 0 V	—	1.75	2.2	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	70	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	600	–	ns
Rise Time	t_r		–	70	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	620	–	ns
Fall Time	t_f		–	60	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 15 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	80	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	600	–	ns
Rise Time	t_r		–	100	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	600	–	ns
Fall Time	t_f		–	70	–	ns

3.4.5. SCM1265MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 A, V_{IN} = 5 V	—	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 20 A,V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	80	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	780	–	ns
Rise Time	t_r		–	120	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1150	–	ns
Fall Time	t_f		–	90	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	85	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	810	–	ns
Rise Time	t_r		–	170	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1100	–	ns
Fall Time	t_f		–	90	–	ns

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3.4.6. SCM1245MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 A, V_{IN} = 5 V	—	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 20 A,V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	75	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	695	–	ns
Rise Time	t_r		–	95	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	675	–	ns
Fall Time	t_f		–	55	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	115	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	715	–	ns
Rise Time	t_r		–	135	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	670	–	ns
Fall Time	t_f		–	50	–	ns

3.4.7. SCM1256MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, V_{IN} = 5 V	—	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 30 A,V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	70	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	760	–	ns
Rise Time	t_r		–	130	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1260	–	ns
Fall Time	t_f		–	90	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	80	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	770	–	ns
Rise Time	t_r		–	160	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	1200	–	ns
Fall Time	t_f		–	90	–	ns

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3.4.8. SCM1246MF

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	–	–	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, V_{IN} = 5 V	–	1.7	2.2	V
Emitter-to-Collector Diode Forward Voltage	V_F	I_F = 30 A, V_{IN} = 0 V	–	1.9	2.4	V
High-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	60	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	660	–	ns
Rise Time	t_r		–	110	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	700	–	ns
Fall Time	t_f		–	50	–	ns
Low-side Switching						
Emitter-to-Collector Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, inductive load, V_{IN} = 0→5 V or 5→0 V, T_j = 25°C	–	70	–	ns
Turn-On Delay Time	$t_{d(on)}$		–	660	–	ns
Rise Time	t_r		–	150	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	690	–	ns
Fall Time	t_f		–	50	–	ns

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4. Mechanical Characteristics

Characteristics	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	See footnote below.*	0.588	—	0.784	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	200	μm	
Package Weight		—	11.8	—	g	

* When mounting a heatsink, it is recommended to use a metric screw of M3 and a plain washer of 7 mm (φ) together at each end of it. See Section 13.2 for more details about screw tightening.

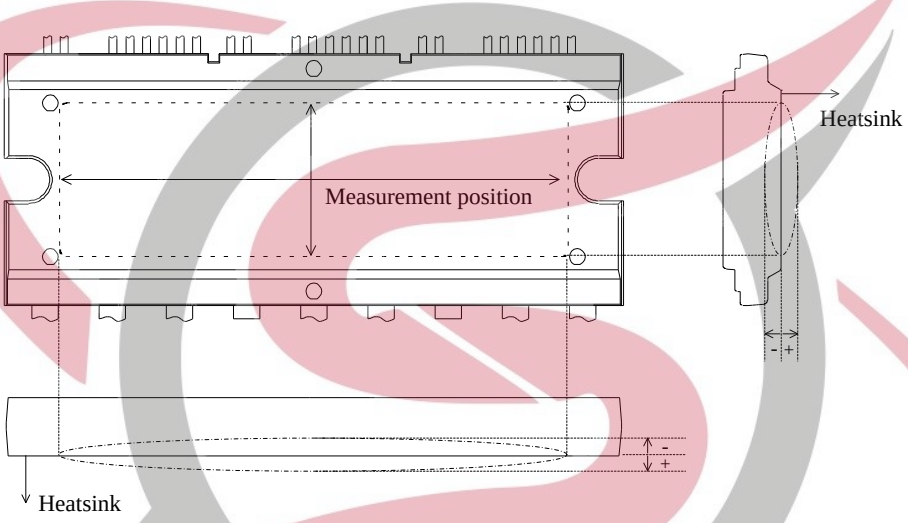

Figure 4-1. Flatness measurement position

5. Insulation Distance

Characteristics	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	2.0	—	2.5	mm	
Creepage		3.86	—	4.26	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

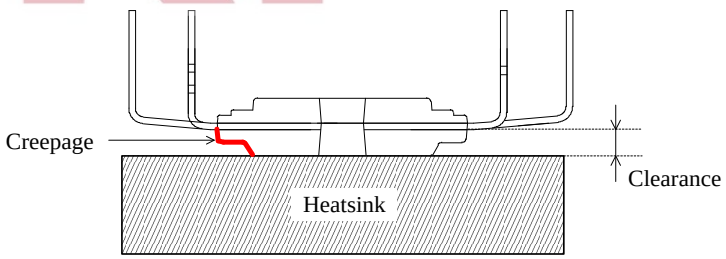

Figure 5-1. Insulation distance definition

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6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HIN and LIN signals in each phase are high at the same time, the simultaneous on-state prevention function sets both the high-side and low-side transistors off.

After recovering from a UVLO_VCC condition, the high-side and low-side transistors resume switching according to the input logic levels of the next HIN and LIN signals (level-triggered).

After recovering from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HIN signal (edge-triggered).

Table 6-1. Truth table for operation modes

Mode	HIN	LIN	High-side Transistors	Low-side Transistors
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
External Shutdown Signal Input FO = L	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
High-side Undervoltage Lockout for Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	OFF
Low-side Undervoltage Lockout for Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF

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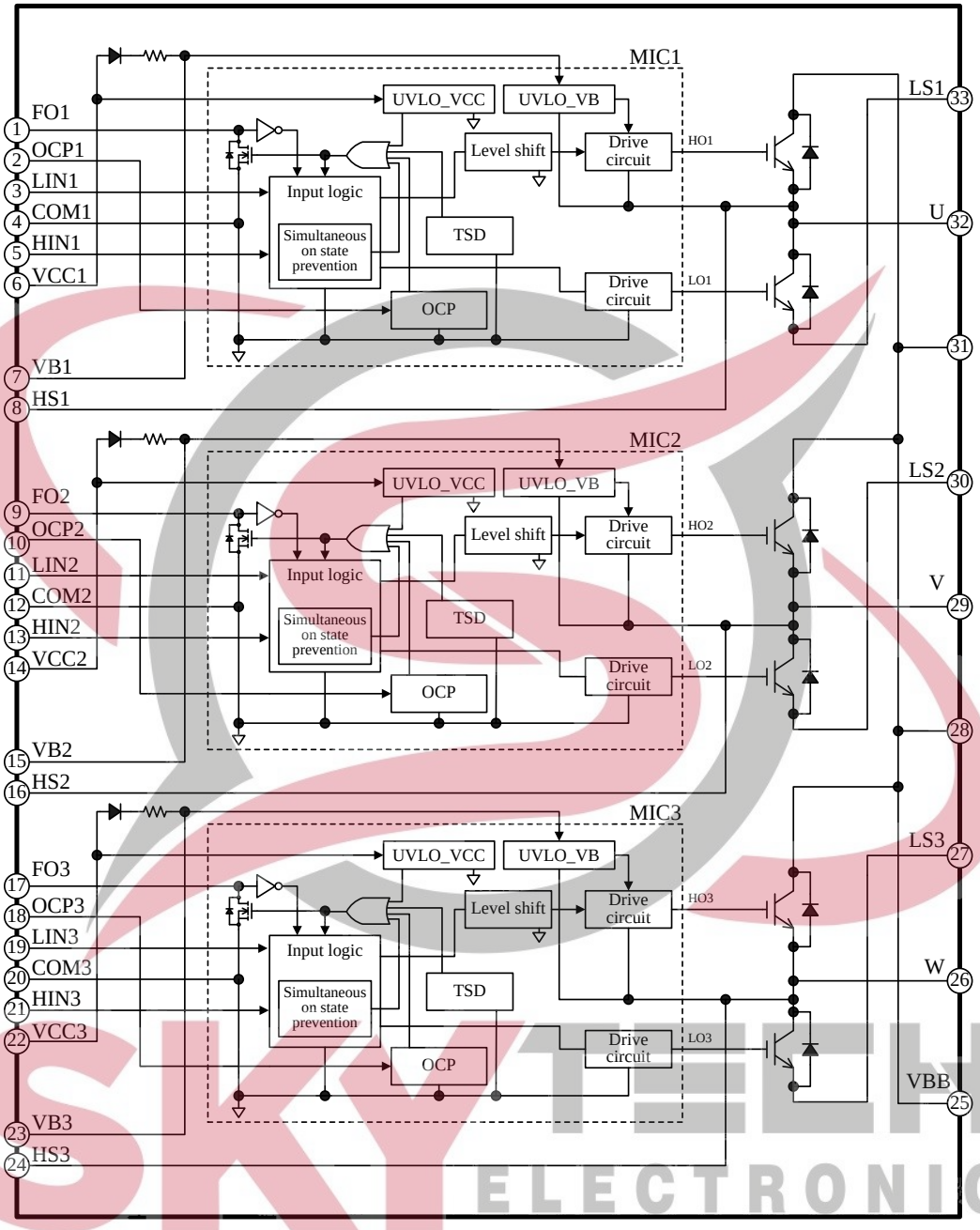
7. Block Diagram



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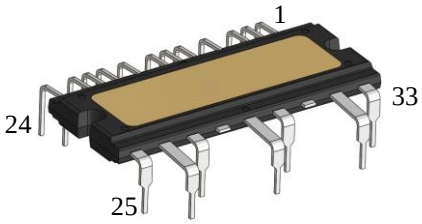
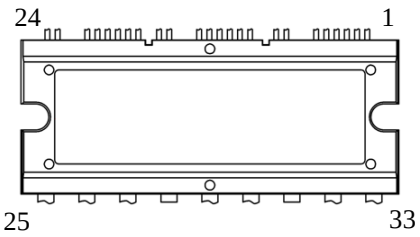
8. Pin-out Diagram



Top view



Pin Number	Pin Name	Functions
1	FO1	U-phase fault output and shutdown signal input
2	OCP1	Input for U-phase Overcurrent Protection
3	LIN1	Logic input for U-phase low-side gate driver
4	COM1	U-phase logic ground
5	HIN1	Logic input for U-phase high-side gate driver
6	VCC1	U-phase logic supply voltage input
7	VB1	U-phase high-side floating supply voltage input
8	HS1	U-phase high-side floating supply ground
9	FO2	V-phase fault output and shutdown signal input
10	OCP2	Input for V-phase Overcurrent Protection
11	LIN2	Logic input for V-phase low-side gate driver
12	COM2	V-phase logic ground
13	HIN2	Logic input for V-phase high-side gate driver
14	VCC2	V-phase logic supply voltage input
15	VB2	V-phase high-side floating supply voltage input
16	HS2	V-phase high-side floating supply ground
17	FO3	W-phase fault output and shutdown signal input
18	OCP3	Input for W-phase Overcurrent Protection
19	LIN3	Logic input for W-phase low-side gate driver
20	COM3	W-phase logic ground
21	HIN3	Logic input for W-phase high-side gate driver
22	VCC3	W-phase logic supply voltage input
23	VB3	W-phase high-side floating supply voltage input
24	HS3	W-phase high-side floating supply ground
25	VBB	Positive DC bus supply voltage
26	W	W-phase output
27	LS3	W-phase IGBT emitter
28	VBB	(Pin trimmed) positive DC bus supply voltage
29	V	V-phase output
30	LS2	V-phase IGBT emitter
31	VBB	(Pin trimmed) positive DC bus supply voltage
32	U	U-phase output
33	LS1	U-phase IGBT emitter

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9. Typical Applications

CR filters and Zener diodes should be added to your application as needed, so that you can: protect each pin against surge voltages causing malfunctions; and avoid the IC being used under the conditions exceeding the absolute maximum ratings, resulting in critical damage to itself. Then test all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

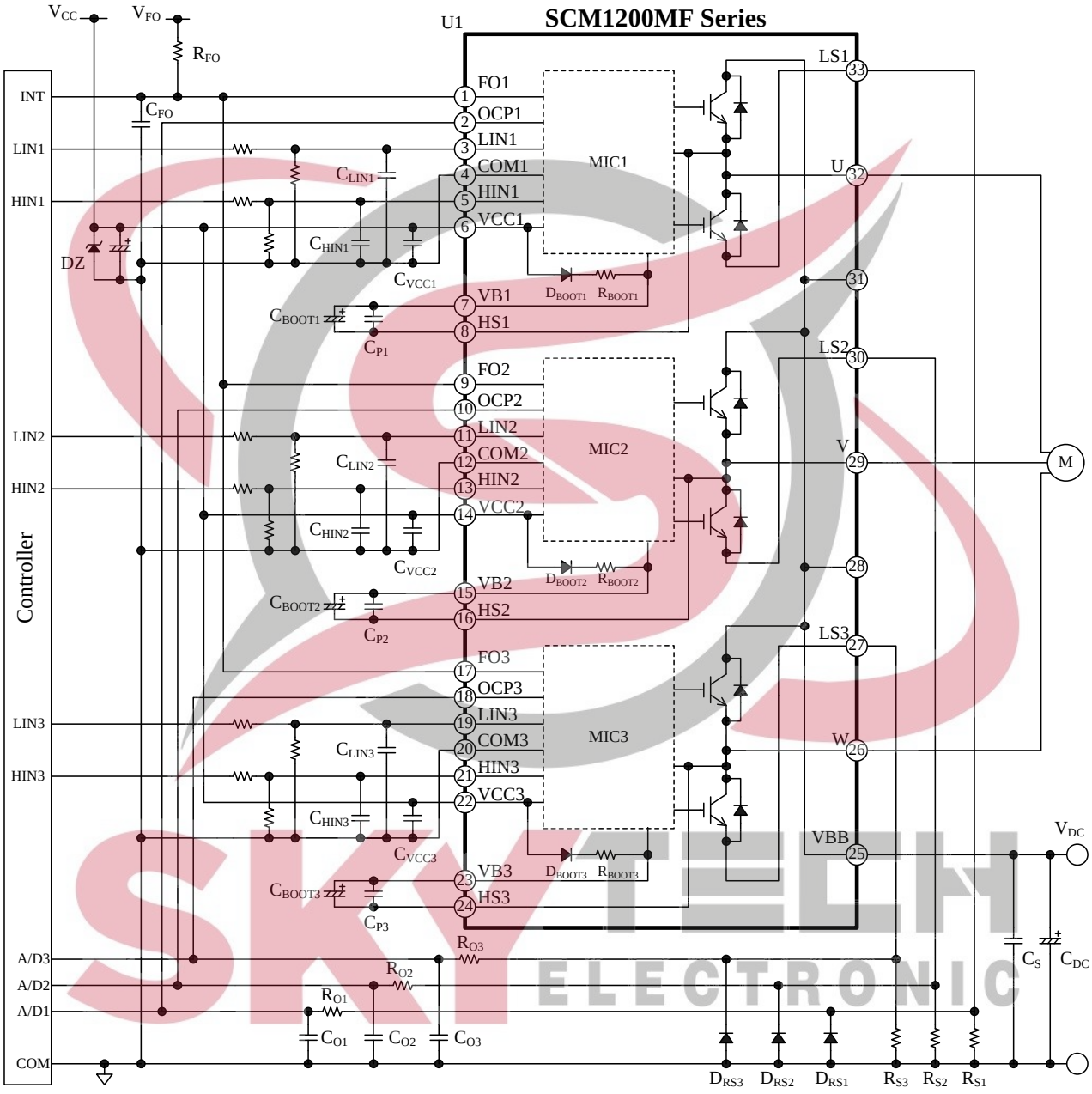

Figure 9-1. Typical application using three shunt resistors

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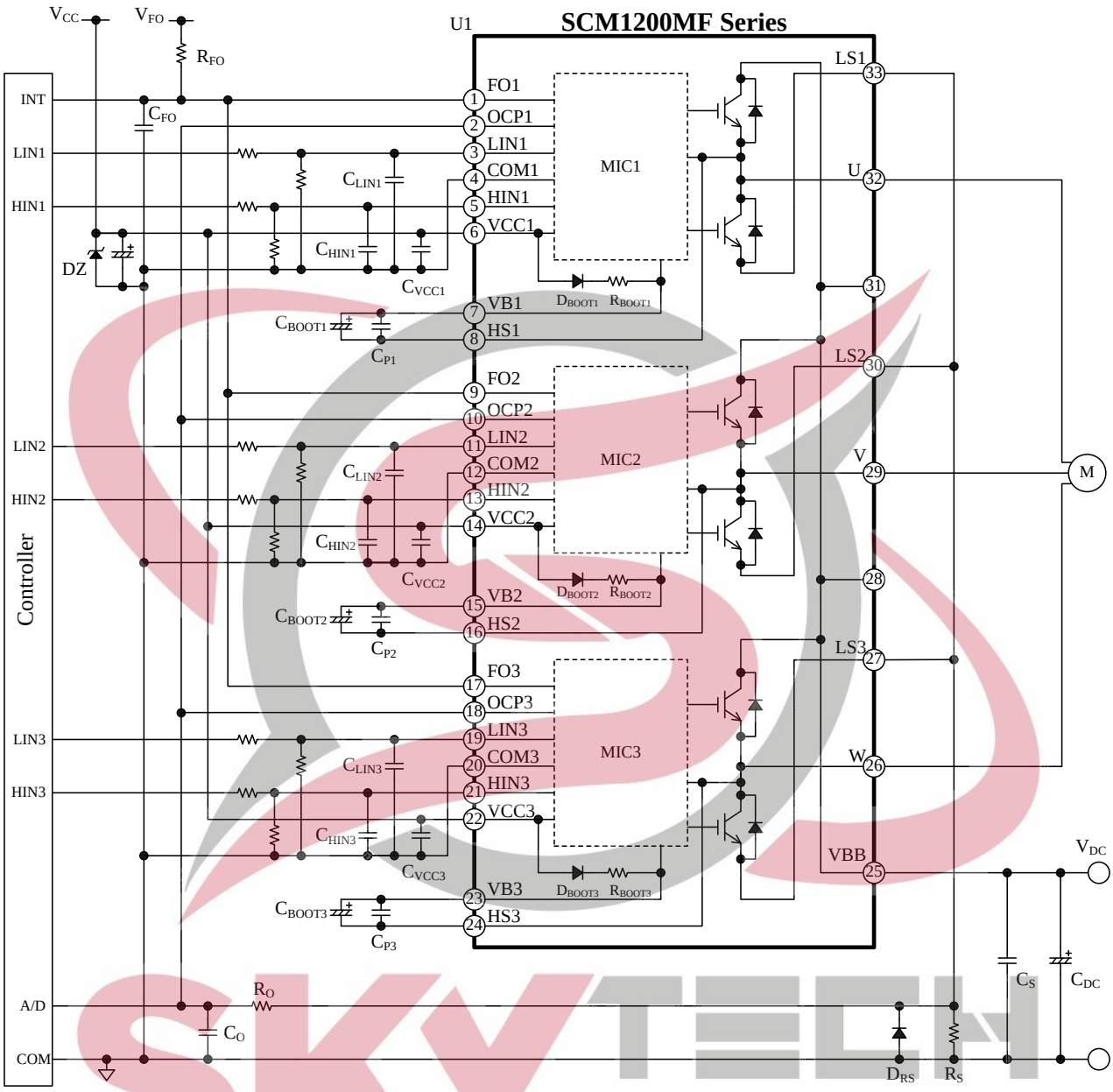

Figure 9-2. Typical application using shingle shunt resistor

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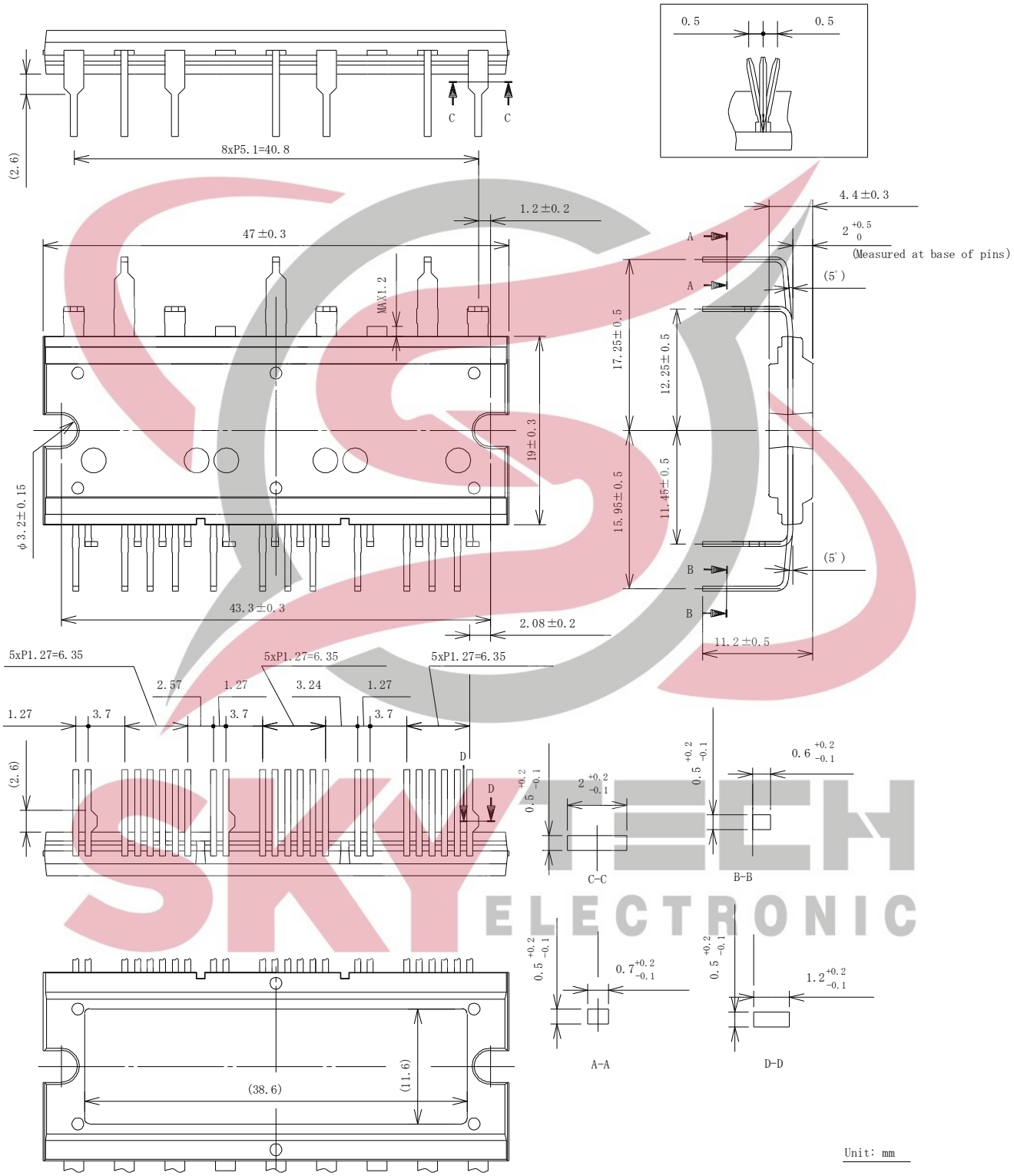
10. External Dimensions

10.1. LF2552



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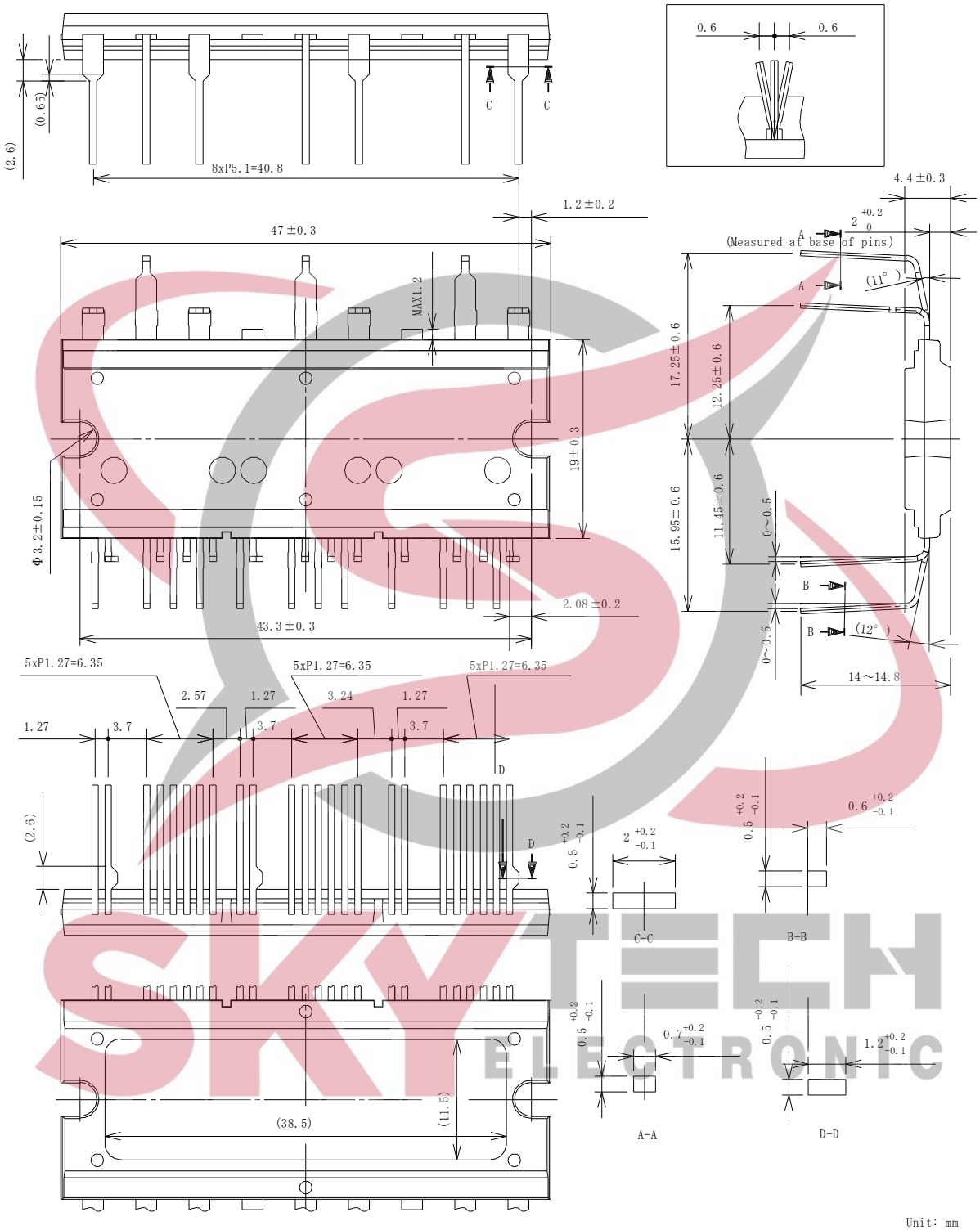
10.2. LF2557 (Long Lead Type)



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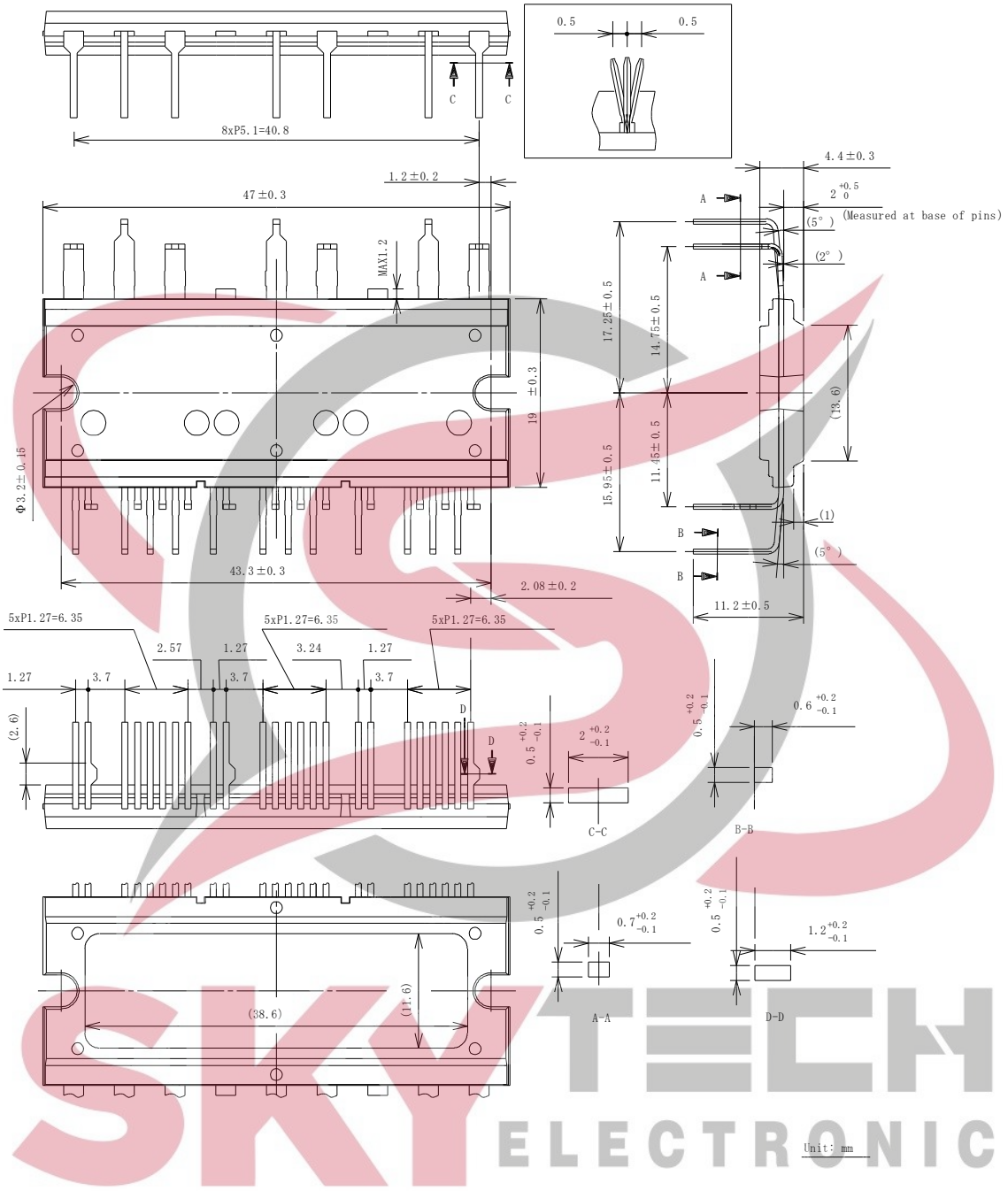
10.3. LF2558 (Wide Lead-Forming Type)



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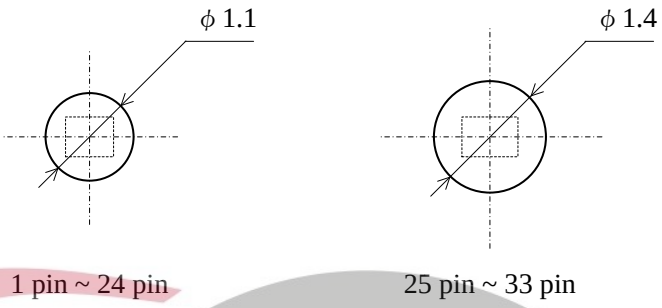
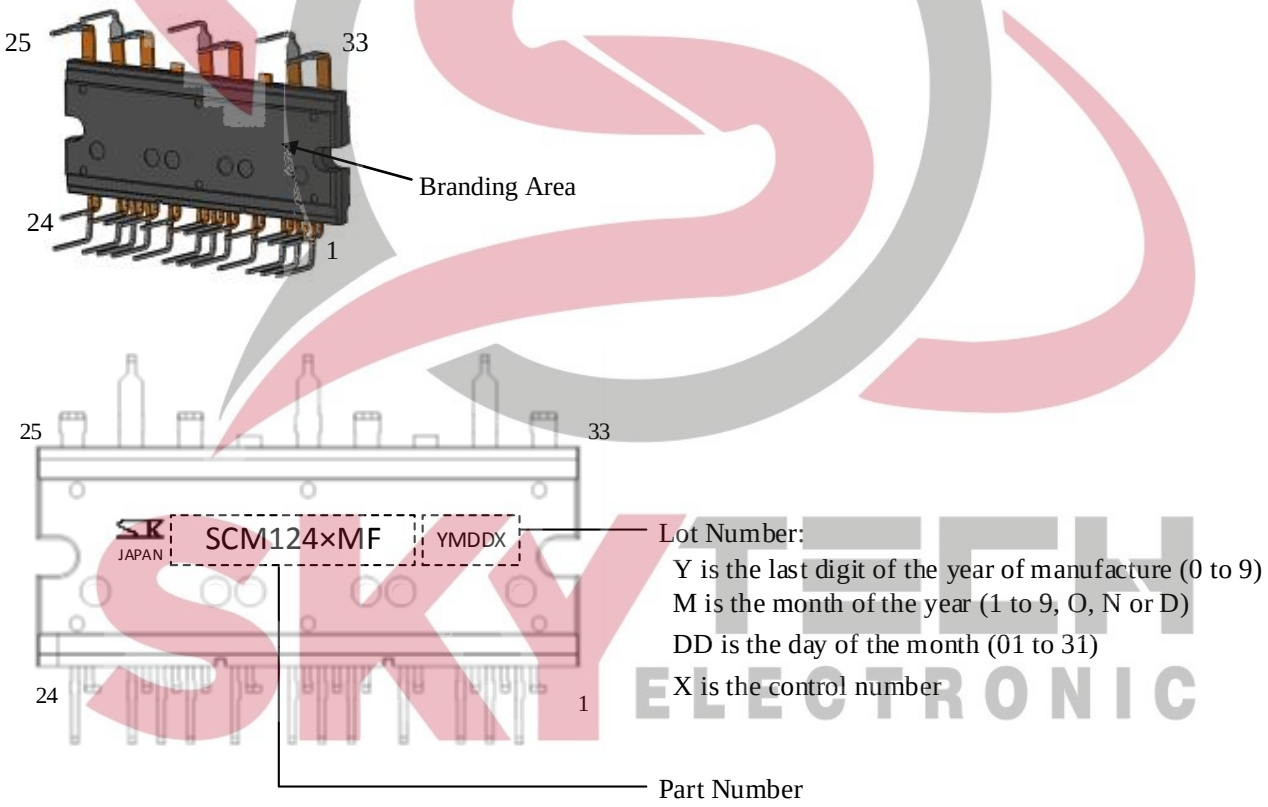
10.4. Recommended PCB Hole Size



11. Marking Diagram



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12. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

For pin descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. The U, V, and W phases are represented as the pin numbers 1, 2, and 3, respectively. Thus, "(the) VBx pin" is used when referring to either of the VB1, VB2, or VB3 pin. Also, when different pin names are mentioned as a pair (e.g., "the VBx and HSx pins"), they are meant to be the pins in the same phase.

12.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences.

To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the logic power supply, V_{CC}, has reached a stable state ($V_{CC(ON)} \geq 12.5$ V). It is required to charge bootstrap capacitors, C_{BOOT}, up to full capacity at startup (see Section 12.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

12.2. Pin Descriptions

12.2.1. U, V, and W

These pins are the outputs of the three phases, and serve as connection terminals to the three-phase motor.

The U, V, and W pins are internally connected to the HS1, HS2, and HS3 pins, respectively.

12.2.2. VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases.

Voltages across the VBx and HSx pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

In each phase, a bootstrap capacitor, C_{BOOT}, should be connected between the VBx and HSx pins.

For proper startup, turn on the low-side transistor first, then charge the bootstrap capacitor, C_{BOOT}, up to its maximum capacity.

Satisfying the formulas below can provide optimal capacitance for the bootstrap capacitors, C_{BOOT}. Note that whichever resulting value is larger should be chosen in order to deal with capacitance tolerance and DC bias characteristics.

$$C_{BOOT}(\mu F) > 800 \times T_{L(OFF)}\ (s) \quad (1)$$

$$10\ \mu F \leq C_{BOOT} \leq 220\ \mu F \quad (2)$$

In Formula (1), let $T_{L(OFF)}$ be the maximum off-time of the low-side transistor, measured in seconds, with the charging time of C_{BOOT} excluded.

Even during the high-side transistor is not on, voltage on the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 12.3.3.1). Therefore, actual board testing should be done thoroughly to validate that voltage across the VBx pin maintains over 12.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As shown in Figure 12-1, in each phase, a bootstrap diode, D_{BOOT}, and a current-limiting resistor, R_{BOOT}, are placed in series between the VCCx and the VBx pins.

The charging time of C_{BOOT}, t_C, is given by Formula (3):

$$t_C = C_{BOOT} \times R_{BOOT}\ , \quad (3)$$

where C_{BOOT} is the optimized capacitance of the bootstrap capacitor, and R_{BOOT} is the resistance of the current-limiting resistor (22 Ω ± 20 %).

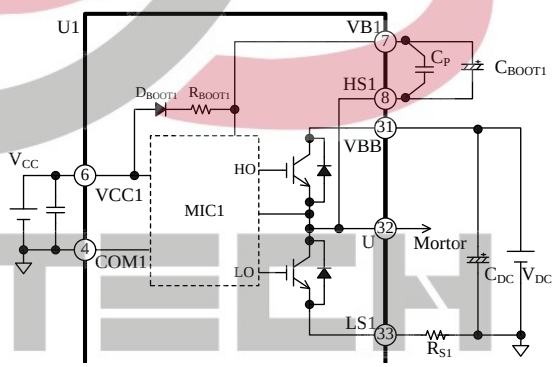

Figure 12-1. Bootstrap circuit

Figure 12-2 shows an internal level-shifting circuit that produces high-side output signals, HOx. A high-side output signal, HOx, begins to respond when an input signal, HINx, transits from low to high (rising edge) or high to low (falling edge). And a signal triggered on a rising edge is called "Set", whereas a signal triggered on a falling edge is called "Reset". Either of these two signals, Set or Reset, is then transmitted to the high-side by the level-shifting circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the

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level-shifting process. When a sharp voltage drop, which is affected by noise, between the VBx and HSx pins (also denoted as "VBx–HSx" in the tables in previous sections), occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of the high-side output, HOx, stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high, the next LINx signal can still turn on the low-side transistor and cause a simultaneously-on condition which may result in critical damage to the IC.

To protect the VBx pin against such noise effect, add a bootstrap capacitor, C_{BOOT}, in each phase. C_{BOOT} should be placed near the IC and connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_P, in parallel near other functional pins used for the same phase.

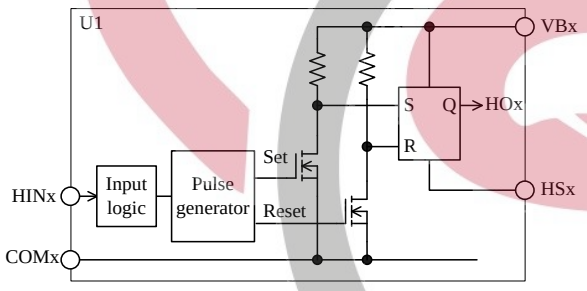

Figure 12-2. Internal level-shifting circuit

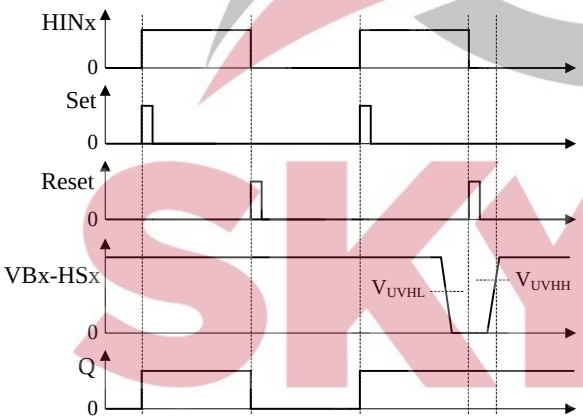

Figure 12-3 Waveforms at VBx–HSx voltage drop

12.2.3. HS1, HS2, and HS3

These pins are the grounds of the high-side floating supplies for each phase, and are connected to negative nodes of the bootstrap capacitors, C_{BOOT}.

The HS1, HS2, and HS3 pins are internally connected to the U, V, and W pins, respectively.

12.2.4. VCC1, VCC2, and VCC3

These are the logic supply pins for the built-in pre-driver ICs. The VCC1, VCC2, and VCC3 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCC}, near other functional pins used for the same phase. To prevent damage caused by surge voltages, put a 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

12.2.5. COM1, COM2, and COM3

These are the logic ground pins for the built-in pre-driver ICs. For proper control, each of them must be connected to the corresponding ground pin. The COM1, COM2, and COM3 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of ground can be a cause of improper operations; therefore, each connection point of these pins should be as close to the LSx pin as possible but separated from the power ground. Moreover, extreme care should be taken when wiring so that currents from the power ground do not affect the COMx pin. To reduce noise effects, connect these pins closely to shunt resistors, R_S, at a single-point ground (or, a star ground) with traces of a minimal length (see Figure 12-4).

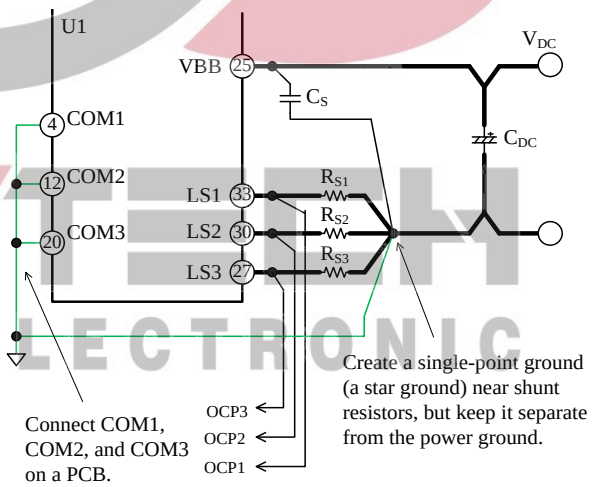

Figure 12-4. Connections to ground pin

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12.2.6. HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller, whereas the LINx pin acts as a low-side controller.

Figure 12-5 shows an internal circuit diagram of the HINx or LINx pin.

This is a CMOS Schmitt trigger circuit with 22 kΩ pull-down resistor and input logic is active high.

Input signals through the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 12-1, below. Note that dead time setting must be done because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures can have sufficient margins in the absolute maximum ranges specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, control the outputs from the microcontroller output line should not be high impedance.

Also, if the traces between the microcontroller and both the HINx and LINx pins are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the the HINx or LINx pin as needed. (See Figure 12-6.

Here are filter circuit constants for reference:

R_{IN1}: 33 Ω to 100 Ω
R_{IN2}: 1 kΩ to 10 kΩ
C_{IN}: 100 pF to 1000 pF

Extra attention should be paid when adding R_{IN1} and R_{IN2} to the traces. When they are connected each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-1. Input signals for HINx and LINx pins

Parameter	"H" Level Signal	"L" Level Signal
Input Voltage	3 V<V_{IN}< 5.5 V	0 V <V_{IN}< 0.5 V
Input Pulse Width	≥ 0.5 µs	≥ 0.5 µs
PWM Carrier Frequency	≤ 20kHz	
Dead Time	≥ 1.0 µs ≥ 1.5 µs (SCM1242MF、SCM1250M)	

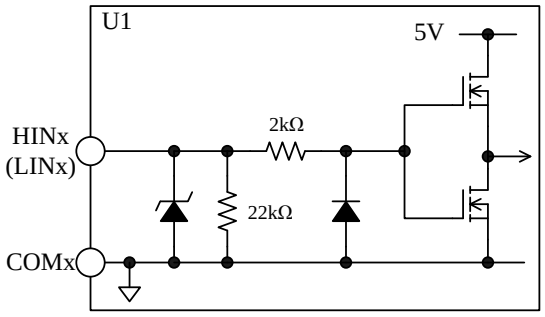

Figure 12-5. Internal circuit diagram of HINx or LINx pin

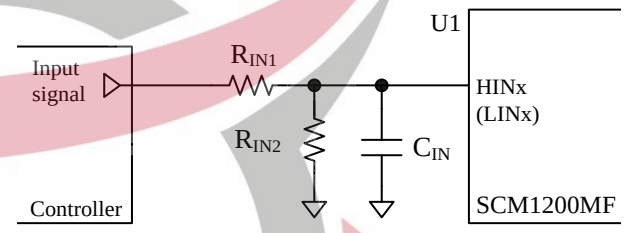

Figure 12-6. Filter circuit for HINx or LINx pin

12.2.7. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this terminal.

Voltages between the VBB and COMx pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To absorb surge voltages, put a 0.01 µF to 0.1 µF snubber capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

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12.2.8. LS1, LS2, and LS3

These are emitter pins of the low-side IGBTs. The LS1, LS2, and LS3 pins are connected to the shunt resistors, R_S.

When connecting shunt resistors to these pins, such as for current detection, trace lengths from the shunt resistors to the IC should be as short as practicable. Otherwise, malfunctioning may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations.

For applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx and COMx pins in order to prevent the IC from malfunctioning.

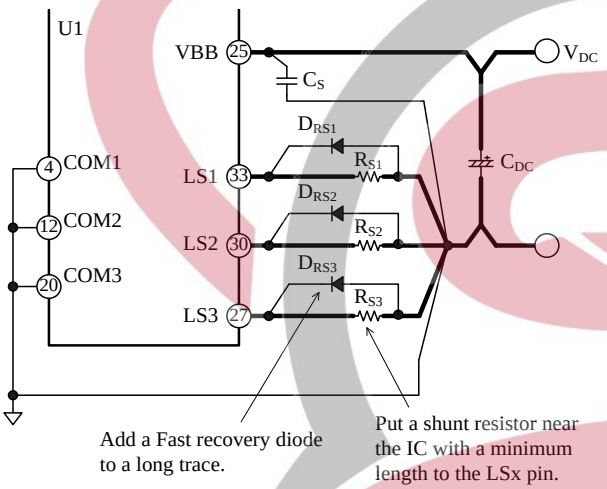

Figure 12-7. Connections to LS pin

12.2.9. OCP1, OCP2, and OCP3

These pins serve as the inputs of the Overcurrent Protection (OCP) for the currents go through output transistors.

Section 12.3.4 provides further information about the OCP circuit configuration and its mechanism.

12.2.10. FO1, FO2, and FO3

These pins operate as fault signal outputs and shutdown signal inputs for each of the three phases.

Sections 12.3.1 and 12.3.2 explain these two functions in detail, respectively.

Figure 12-8 illustrates a schematic diagram of the FOx pin and its peripheral circuit. Because of its open-drain nature, each of the FOx pins should be tied by a pull-up resistor, R_{FO}, to external power supply voltage, V_{FO}. The external power supply voltage, V_{FO}, should range from 3.0 V to 5.5 V.

Figure 12-10 shows a relation between the FOx pin voltage and a pull-up resistance value. When a pull-up resistor, R_{FO}, has a too small resistance value, the FOx pin voltage at fault signal output becomes high due to the on-resistance of a built-in MOSFET, Q_{FO} (Figure 12-8). Therefore, it is recommended to use a 1 kΩ to 22 kΩ pull-up resistor when the low-level input threshold voltage of a microcontroller, V_{IL}, is set to 1.0 V.

To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FOx and COMx pins. Note that, however, this additional filtering allows a delay time, $t_{D(FO)}$, to occur, as shown in Figure 12-9. The delay time, $t_{D(FO)}$, is a period of time which starts when the IC receives a fault flag turning on the internal MOSFET, Q_{FO}, and continues until when the FOx pin reaches its threshold voltage (V_{IL}) of 1.0 V or below (put simply, until the time when the IC detects a logic low state, "L").

Figure 12-11 shows how the delay time, $t_{D(FO)}$, and the noise filter capacitor, C_{FO}, are related.

To avoid the repetition of Overcurrent Protection (OCP) activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, which occurs after the MOSFET (Q_{FO}) turn-on. t_P is 15 µs where minimum values of temperature characteristics are taken into account. (For more details, see Section 12.3.4.)

When V_{IL} is set to 1.0 V, it is recommended to use a 0.001 µF to 0.01 µF noise filter capacitor, C_{FO}, allowing a sufficient margin to deal with variations in characteristics.

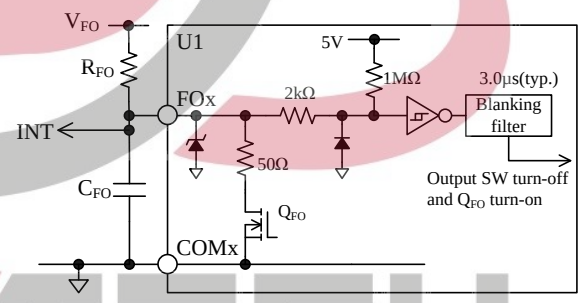

Figure 12-8. Internal circuit diagram of FOx pin and its peripheral circuit

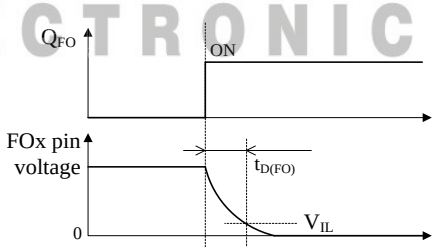

Figure 12-9. FOx pin delay time, $t_{D(OFF)}$

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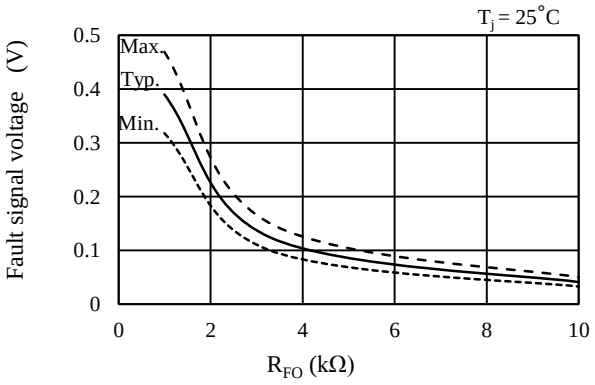

Figure 12-10. Fault signal voltage vs. pull-up resistor value, R_{FO}

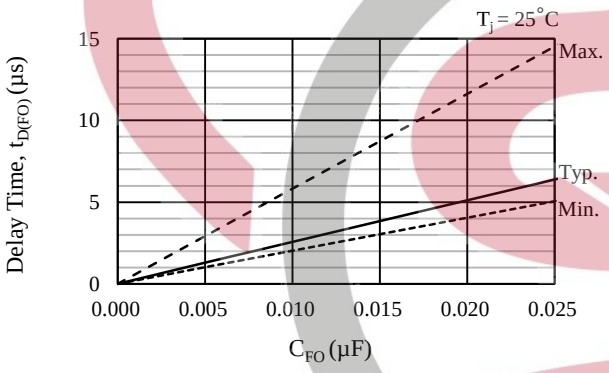

Figure 12-11. Delay time, $t_{D(FO)}$ vs. filter capacitor, C_{FO}

12.3. Protection Functions

This section describes the various protection circuits provided in the SCM1200MF series.

The protection circuits include: the undervoltage lockout for power supply (UVLO), the simultaneous on-state prevention function, the overcurrent protection (OCP), and the thermal shutdown (TSD).

In case one or more of these protection circuits are activated, the FO pin outputs a fault signal and the external microcontroller stops all operations of the three phases. The external microcontroller can also shut down the IC operations by inputting a fault signal to the FOx pin.

In the following function descriptions, "HOx" denotes a gate input signal on the high-side transistor; whereas "LOx" denotes a gate input signal on the low-side transistor (See also the diagrams in Section 7.). "VBx–HSx" refers to the voltages between the VBx pin and HSx pin.

12.3.1. Fault Signal Output

In case one or more of the following protections are actuated, internal MOSFET, Q_{FO}, turns on and the FOx pin becomes to logic low (≤ 0.5 V).

1) Low-side undervoltage lockout (UVLO_VCC)
2) Overcurrent protection (OCP)
3) Simultaneous on-state prevention
4) Thermal shutdown (TSD)

During the time when the FOx pin holds the logic low state, the high- and low-side transistors of each phase turn off. In normal operation, the FOx pin holds an "H" state and outputs a 5 V signal.

The fault signal output time of the FOx pin at OCP activation is OCP hold time (t_P) of 26 µs (typ.), fixed by a built-in feature of the IC itself (see Section 12.3.4). The fault signals are then sent to an interrupt pin (INT) of the external microcontroller, and should be processed as an interrupt task to be done within the predetermined OCP hold time, t_P.

12.3.2. Shutdown Signal Input

The FO1, FO2, and FO3 pins also can be the input pins of shutdown signals. When the FOx pin becomes logic low, the high- and low-side transistors of each phase turn off.

The voltages and pulse widths of the shutdown signals to be applied between the FOx and COMx pins are listed in Table 12-2.

Table 12-2. Shutdown signals

Parameter	"H" Level Signal	"L" Level Signal
Input Voltage	3 V < V_{IN}< 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥ 0.5 µs	≥ 0.5 µs

In Figure 12-12, FO1, FO2 and FO3 are all connected. If an abnormal condition is detected by either one of the MICs, the high- and low-side transistors of all phases can be turned off at once.

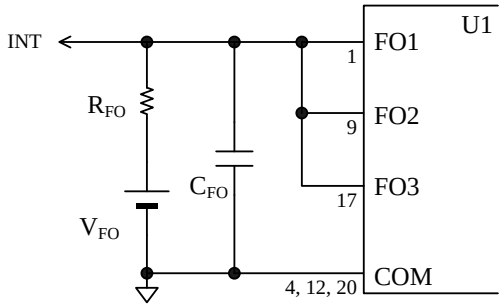

Figure 12-12. All-phase shutdown circuit

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12.3.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltage of output transistors decreases, the steady-state power dissipation of the transistors increases and the IC may have permanent damage, in the worst case. To prevent this event, the SCM1200MF series has the undervoltage lockout (UVLO) circuit for both of the high- and low-side power supplies in each controller IC (MIC).

12.3.3.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 12-13 shows operational waveforms of the undervoltage lockout operation for high-side power supply (i.e., UVLO_VB).

When the voltage between the VBx and HSx pins (VBx–HSx) decreases to the Logic Operation Stop Voltage of high-side ($V_{BS(OFF)}$, 11.0 V), the UVLO_VB circuit in the corresponding phase activates and sets only HOx signals to logic low. When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage of high-side ($V_{BS(ON)}$, 11.5 V), the IC releases the UVLO_VB condition. Then, the HOx signals become logic high at the rising edge of the first input command after the UVLO_VB release.

The FOx pin does not transmit any fault signals during the UVLO_VB activation. In addition, each of the VBx pins has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

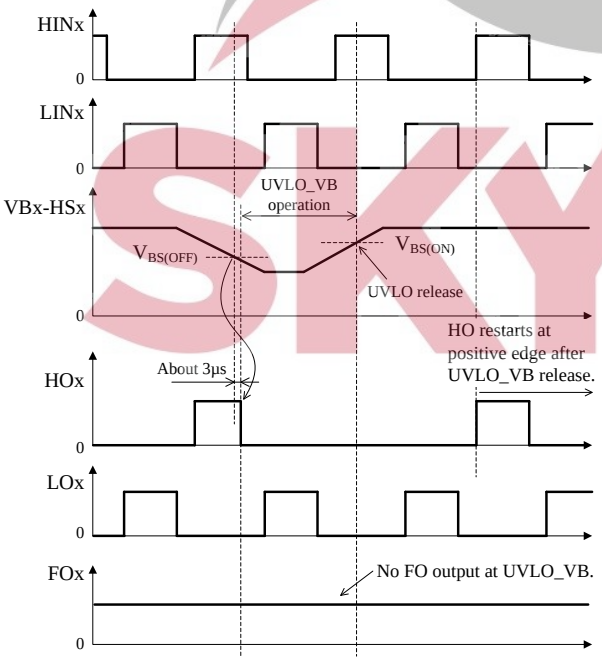

Figure 12-13. Operational waveforms of UVLO_VB

12.3.3.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 12-14 shows operational waveforms of the undervoltage lockout operation for low-side power supply (i.e., UVLO_VCC).

When the VCCx voltage decreases to the Logic Operation Stop Voltage of low-side ($V_{CC(OFF)}$, 11.0 V), the UVLO_VCC circuit in the corresponding phase activates and sets both of HOx and LOx signals to logic low.

When the VCCx voltage increases to the Logic Operation Start Voltage of low-side ($V_{CC(ON)}$, 11.5 V), the IC releases the UVLO_VCC condition. Then it resumes transmitting HOx and LOx signals according to the input commands on the HINx and LINx pins.

The FOx pin becomes logic low during the UVLO_VCC activation.

In addition, each of the VCCx pins has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

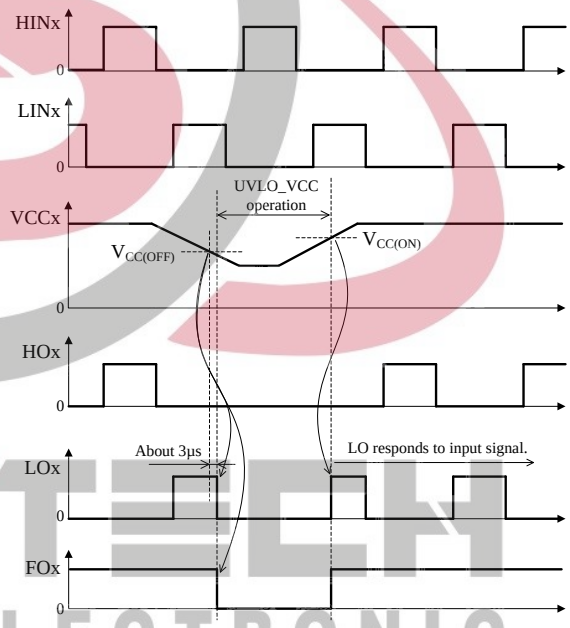

Figure 12-14. UVLO_VCC operational waveforms

12.3.4. Overcurrent Protection (OCP)

Figure 12-15 shows an internal circuit diagram of the OCPx pin, and OCPx pin peripheral circuitry.

The OCPx pin detects overcurrents with input voltage across external shunt resistor, R_S. Since the OCPx pin is internally pulled-down, the OCPx pin voltage increases proportionally to a rise in the current running through the shunt resistor.

Figure 12-16 is a timing chart that represents

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operation waveforms at OCP. When the OCPx pin voltage increases to an Overcurrent Protection Threshold Voltage, V_{TRIP}, of 0.50 V, and then keeps in that condition for an Overcurrent Protection Blanking Time, t_{BK}, of 1.65 µs or longer, the OCP circuit starts operating. The enabled OCP circuit then shuts off the output transistors and puts the FOx pin into a logic low state. Even if the OCPx pin voltage falls below V_{TRIP}, the IC keeps in a logic low state for a fixed OCP hold time (t_P) of 26 µs (typ.). Then, the output transistors operate according to input signals. Then, the output transistors operate according to input signals.

The OCP circuits in the SCM1200MF series are used for detecting abnormal conditions, such as an output transistor shorted. Therefore, motor operation must be stopped by the external microcontroller, which can receive and handle fault signals from the IC. Otherwise, your application will be more likely to cause short circuit conditions repeatedly, thus the breakdown of the output transistors.

Care should also be taken when using a 3-shunt resistor system in your application. The IC running on the 3-shunt resistor system only shuts off the output transistor in the phase where an overcurrent condition exists. And a fault signal is transmitted from the FOx pin of the phase being under the overcurrent condition.

As already shown in Figure 12-12, if all of the FOx pins being used makes a short circuit, a fault signal sent from the corresponding phase can turn off the output transistors of all phases (see Section 12.3.2).

To place a shunt resistor in an actual application, users must set:

- the shunt resistor to have the resistance specified as shunt resistor, R_S (see the recommended operating condition table, Section 2);
- input voltages of the OCPx pin to keep their levels within the range defined as the OCPx pin voltage, V_{OCP} (see the absolute maximum rating table, Section 1); and
- currents through output transistors to keep their levels under the rated output current (pulsed), I_{OP} (see the absolute maximum rating table, Section 1).

Because high-frequency switching currents flow through the shunt resistors, R_S, choose a resistor that has low inductance and allows high power dissipation.

When adding a CR filter (a pair of a filter resistor, R_O and a filter capacitor, C_O) to the OCPx pin, the following should be taken into account. Time constants of R_O and C_O should be set to the values listed in Table 12-3.

The larger the time constant, the longer the time that the OCPx pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, the time constants given here are determined in consideration of the total delay time the IC will have.

The filter capacitor, C_O, should also be placed near the IC, between the OCPx and COMx pins with a minimal length of traces.

Note that overcurrents are undetectable when one or more of the U, V, and W pins are shorted to ground (ground fault). In case either of these pins falls into a state of ground fault, the transistors may be destroyed.

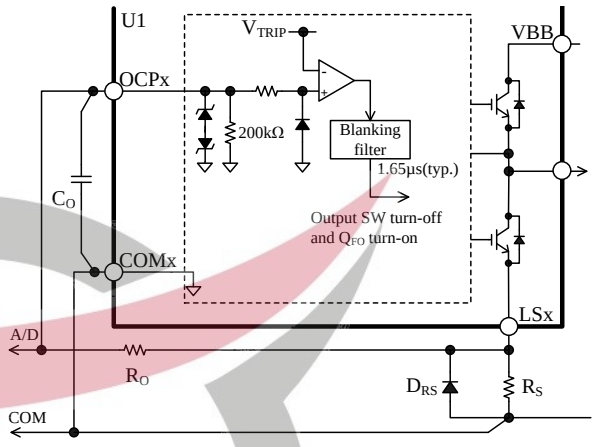

Figure 12-15. Internal circuit diagram of OCPx pin and OCPx pin peripheral circuitry

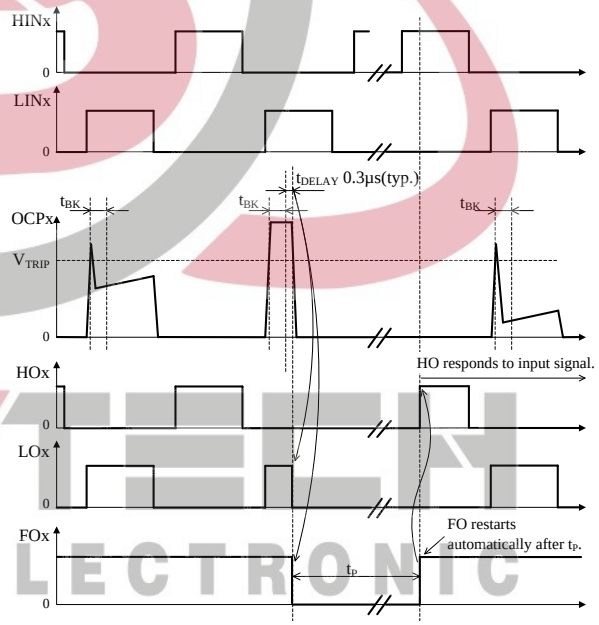

Figure 12-16. OCP operational waveforms

Table 12-3. Recommend time constants for CR filter

Products	Recommend time constants
SCM124×MF SCM125×MF	0.22 µs or less
SCM126×MF	1 µs or less

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12.3.5. Simultaneous On-state Prevention

When both of the HINx and LINx pins receive logic high signals at once, the high- and low-side transistors turn on at the same time, allowing overcurrents to pass through. As a result, the switching transistors will be destroyed. In order to protect this event, the simultaneous on-state prevention circuit is built into each of the controller ICs. Note that incorrect command input and noise interference are also largely responsible for such a simultaneous-on condition.

When logic high signals are asserted on the HINx and LINx pins at once, as shown in Figure 12-17, this function gets activated and turns the high- and low-side transistors off.

Then, the FOx pin becomes a logic low state, and sends fault signals during this function activation.

After the IC comes out of the simultaneous On-state, "HOx" and "LOx" start responding in accordance with HINx and LINx input commands again. In order to prevent malfunctions due to noise, the simultaneous on-state prevention circuitry has a filter of about 0.8 µs.

Note that the function does not have any of dead-time programming circuits. Input signals to the HINx and LIN pins must have proper dead times as defined in Section 0).

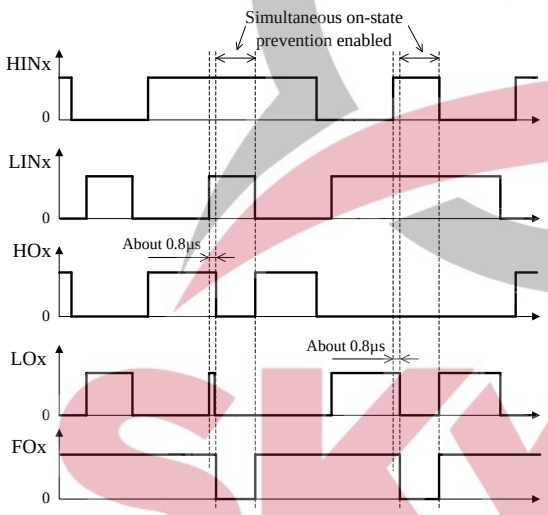

Figure 12-17. Operational waveforms of Simultaneous On-state Prevention

12.3.6. Thermal Shutdown (TSD)

The IC has thermal shutdown (TSD) circuits. Figure 12-18 shows the TSD operational waveforms.

In case of overheating, e.g., increased power dissipation due to overload, or an ambient temperature rise at the device, the IC shuts down the high- and low-side output transistors.

Thermal detection is monitored by the MICs (see Section 7).

When the temperature of the MIC increases to T_{DH} = 150 °C or more, the corresponding TSD circuit is activated. When the temperature decreases to T_{DL} = 120 °C or less, the shut-down condition is released and the transistors resume operating according to input signals.

When the TSD circuits is being enabled, FOx pin becomes logic low and transmits fault signals.

Note that junction temperatures of the output transistors themselves are not monitored. Do not use the TSD function as a prevention function against critical damage to the output transistors.

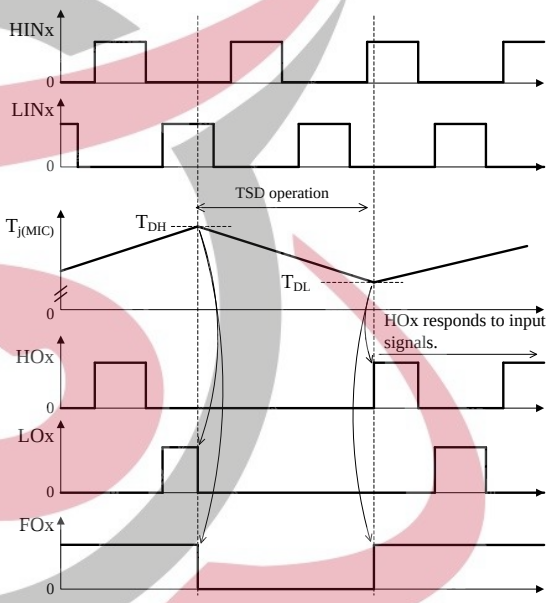

Figure 12-18. TSD operational waveforms

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13. Design Notes

This section also employs the terminal notation system for pin names, described in the beginning of the previous section.

13.1. PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor driver circuit. The motor driver circuit consists of current paths carrying high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation.

Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops which carry high frequencies and high voltages should be as small and wide as you can, in order to maintain a low-impedance state.

In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

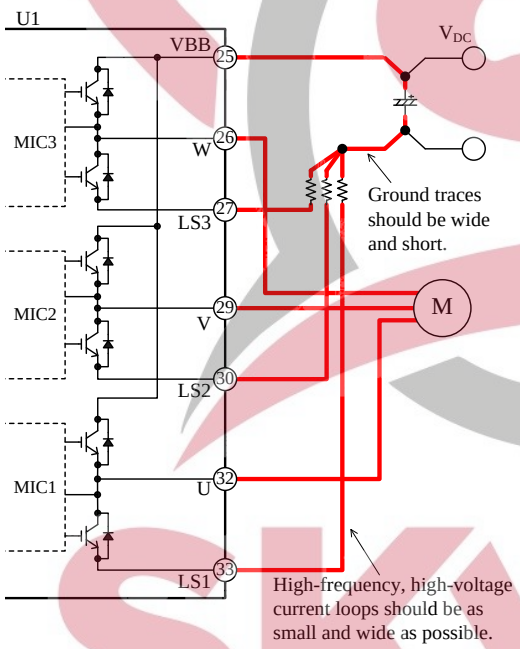

Figure 13-1. High-frequency, high-voltage current paths

13.2. Heatsink Mounting Considerations

This section provides the guidelines for mounting a heatsink, as follows:

- It is recommended to use a pair of a metric screw of M3 and a plain washer of 7 mm (φ).
  Use a torque screwdriver to tighten the screws. Tighten the two screws firstly up to about 30% of the maximum screw torque; then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.
- When mounting a heatsink, it is recommended to use silicone greases.
  If a thermally-conductive sheet or an electrically insulating sheet is used, package cracks may be occured due to creases at screw tightening. Therefore, thorough evaluations should be conducted before using these materials.
- When applying a silicon grease, there must be no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicon grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  – Grease thickness: 100 µm
  – Heatsink flatness: ±100 µm
  – When applying a silicon grease to a heatsink, it should be applied within the area indicated in Figure 13-2, below.

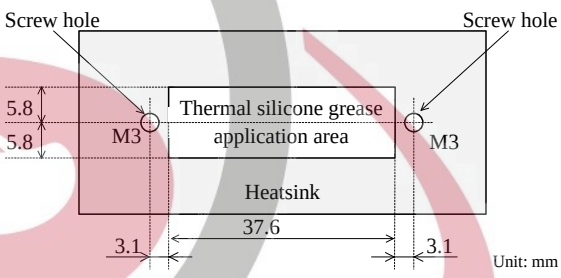

Figure 13-2. Recommended application area for thermal silicone grease

13.3. IC Characteristics Measurement Considerations

When measuring the breakdown voltage and/or leakage current of the transistors incorporated in the IC, the gate and emitter of each transistor should have the same potential.

Moreover, care should be taken because the collectors are all internally connected to the VBB pin.

The output (U, V, and W) pins are connected to the emitters of the corresponding high-side transistors; and the LSx pins are connected to the emitters of the low-side transistors. The gates of the high-side transistors are pulled down to the output (U, V, W) pins; similarly, the gates of the low-side transistors are pulled down to the COMx pins.

Note that the output, LS, and COMx pins must be connected appropriately before measuring breakdown voltage and/or leak current. Otherwise the switching transistors may result in permanent damage.

The figures below are the schematic circuit diagrams of a typical measurement circuit for breakdown voltage: Figure 13-3 shows the high-side transistor (Q_{1H}) in U

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phase, and Figure 13-4 shows the low-side transistor (Q_{1L}) in U phase. And all the pins that are not represented in these figures are open.

Before conducting a measurement, be sure to isolate the ground of a measurement phase from those of other two phases. Then, in each of the two separated phases, connect the LSx and COMx pins each other at the same potential, and leave them unused and floated.

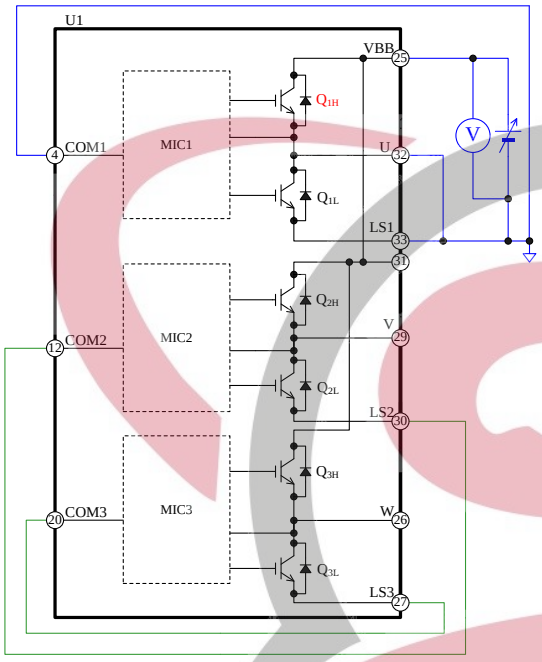

Figure 13-3. Typical measurement circuit of high-side transistor (Q_{1H}) in U phase

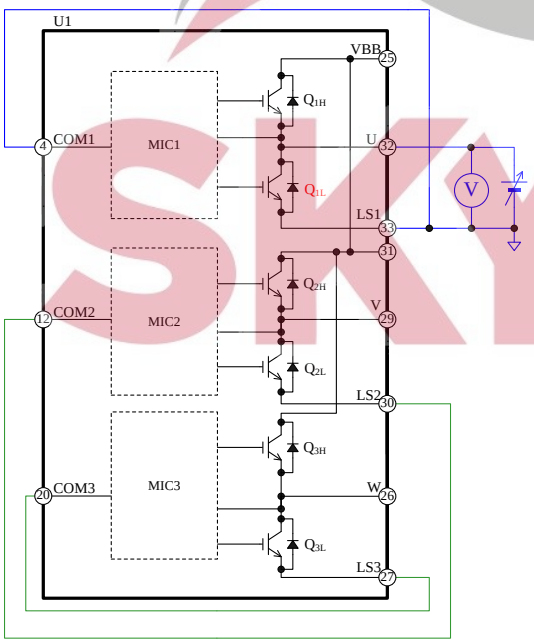

Figure 13-4. Typical measurement circuit of low-side transistor (Q_{1L}) in U phase

14. Calculating Power Losses and Estimating Junction Temperatures

This section describes the procedures to: calculate power losses in a switching transistor; and estimate junction temperatures. Note that the following descriptions are applicable to the SCM1200MF series, which is controlled by a three-phase sine-wave PWM driving strategy.

The total power losses in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}.

The following subsections contain the mathematical procedures to calculate power losses in an IGBT and its junction temperature.

14.1. IGBT Steady-State Loss, P_{ON}

The steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, shown in Section 15.3.1. As shown in Figure 14-1, the following linear approximate equation can be obtained from the curves: $V_{CE(SAT)} = \alpha \times I_C + \beta$. The slope and intercept of the linear approximate equation are used in Formula (4).

Table 14-1 lists the reference slopes and intercepts of the linear approximate equation at a half of output current, 0 to 0.5 × I_O.

The values calculated with the linear approximation greatly differ at the point where I_C is near zero. But in dissipation calculation, the difference is regarded as an error tolerance. Hence, the equation for the steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M. \quad (4)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT in V,
I_C is the collector current of the IGBT in A, and
DT is the on-time duty cycle.

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current in A,
α is the slope of the linear approximate equation in the $V_{CE(SAT)}$ vs. I_C curve, and

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β is the intercept of the linear approximate equation in the $V_{CE(SAT)}$ vs. I_C curve.

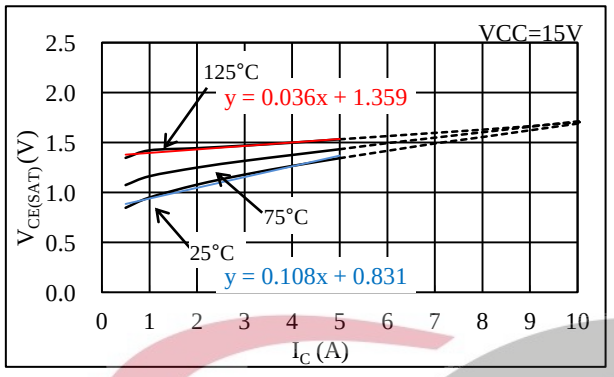

Figure 14-1. Linear approximate equation of $V_{CE(SAT)}$ vs. I_C curve

Table 14-1. Reference slopes (α) and intercepts (β) of linear approximate equation at 0 to 0.5 × I_O in $V_{CE(SAT)}$–I_C curve

Part Number	25°C		125°C	
	α	β	α	β
SCM1261MF	0.108	0.831	0.036	1.359
SCM1242MF SCM1263MF SCM1243MF	0.093	0.694	0.060	0.974
SCM1265MF SCM1245MF	0.043	0.907	0.063	0.702
SCM1256MF SCM1246MF	0.046	0.739	0.031	0.991

14.2. GBT Switching Loss, P_{SW}

The switching loss in an IGBT can be calculated by Formula (5), letting I_M be the effective current value of a motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \left(E_{ON}(I_M) + E_{OFF}(I_M)\right) \times \frac{V_{DC}}{300}, \quad (5)$$

where:

fc is the PWM carrier frequency in Hz,

V_{DC} is the main power supply voltage in V (i.e., the VBB pin input voltage),

$E_{ON}(I_M)$ is the turn-on loss at I_M in J, and

$E_{OFF}(I_M)$ is the turn-off loss at I_M in J.

For $E_{ON}(I_M)$ and $E_{OFF}(I_M)$, see also Section 15.3.2.

14.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT, T_j, can be estimated with Formula (6), below:

$$T_j = R_{(j-C)Q} \times (P_{ON} + P_{SW}) + T_C \,. \quad (6)$$

Where

$R_{(j-c)Q}$ is the junction-to-case thermal resistance of the IGBT product (°C/W), and

T_C is the case temperature (°C), measured at the point shown in Figure 3-1.

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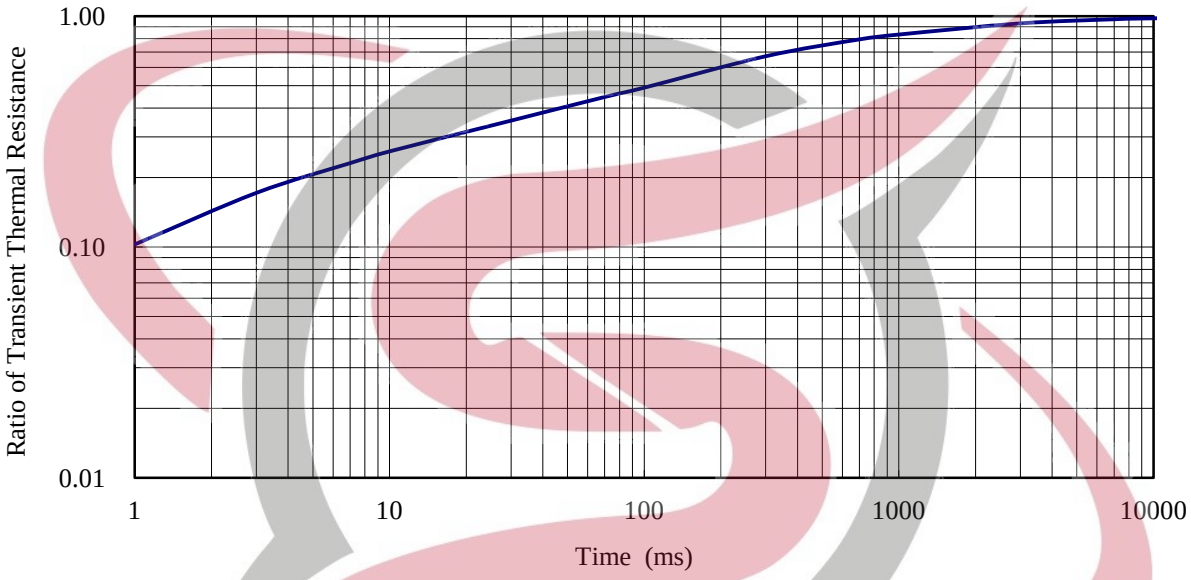
15. Typical Characteristics

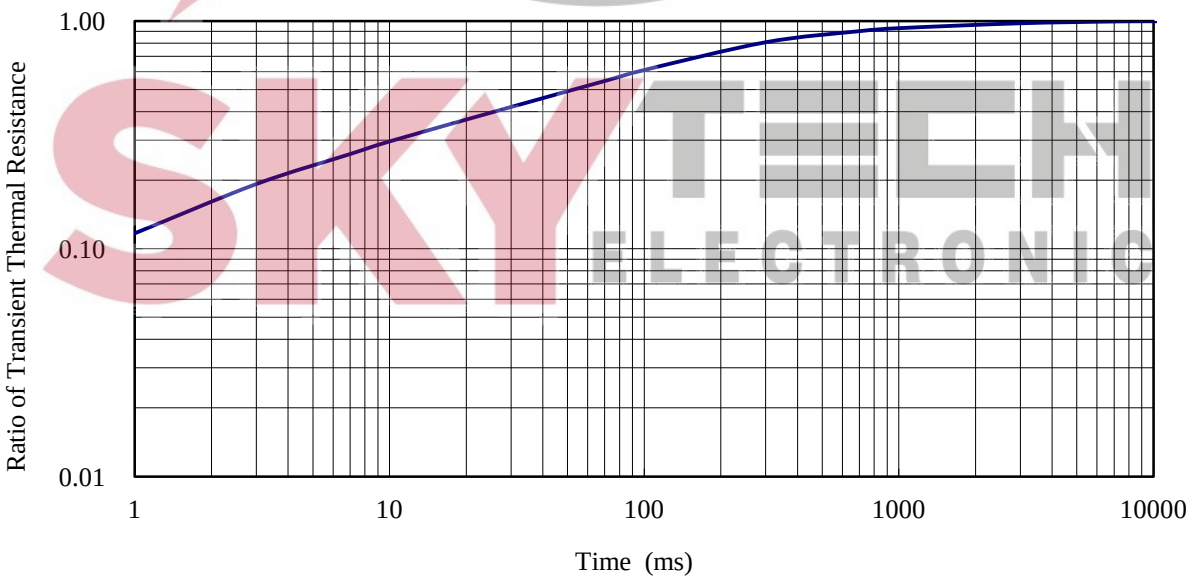
15.1. Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

15.1.1. SCM1261MF



15.1.2. SCM1242MF, SCM1263MF, SCM1243MF



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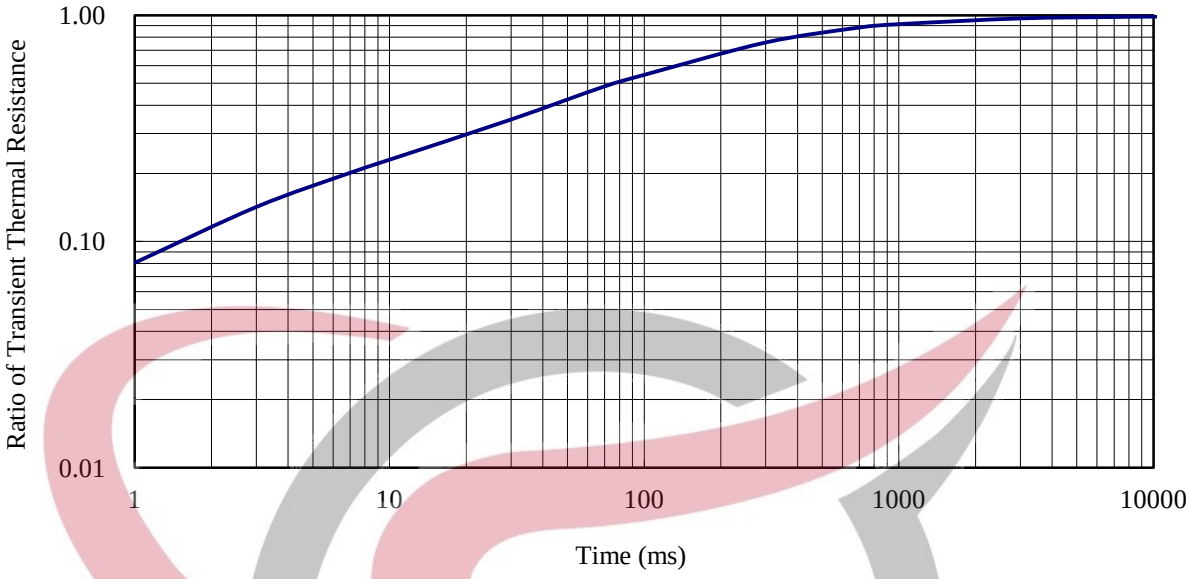
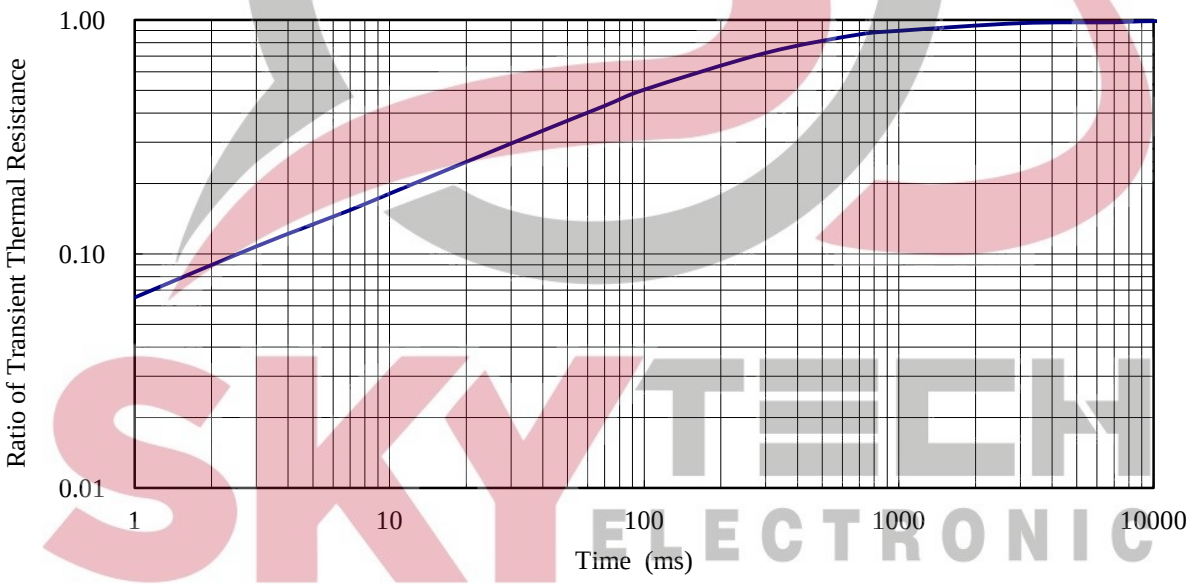
15.1.3. SCM1265MF, SCM1245MF



15.1.4. SCM1246MF, SCM1256MF



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15.2. Performance Curves of Control Parts

Figure 15-1 to Figure 15-26 provide performance curves of the control parts integrated in the SCM1200MF series, including variety-dependent characteristics and thermal characteristics. The term T_j represents the junction temperature of the control parts.

Table 15-1. Typical characteristics of control parts

Figure Number	Figure Caption
Figure 15-1	Logic Supply Current in three-phase operating, ICC vs. Tj
Figure 15-2	Logic Supply Current in three-phase operating, ICC vs. VCCx pin voltage, VCC
Figure 15-3	Logic Supply Current in single-phase operating (HINx = 0 V), IBS vs. Tj
Figure 15-4	Logic Supply Current in single-phase operating (HINx = 5 V), IBS vs. Tj
Figure 15-5	Logic Supply Current in single-phase operating (HINx = 0 V), IBS vs. VBx pin voltage, VB
Figure 15-6	Input Current at High Level (HINx or LINx) vs. Tj
Figure 15-7	High Level Input Signal Threshold Voltage, VIH vs. Tj
Figure 15-8	Low Level Input Signal Threshold Voltage, VIL vs. Tj
Figure 15-9	High-side turn-on propagation delay vs. Tj (from HINx to HOx)
Figure 15-10	High-side turn-off propagation delay vs. Tj (from HINx to HOx)
Figure 15-11	Low-side turn-on propagation delay vs. Tj (from LINx to LOx)
Figure 15-12	Low-side turn-off propagation delay vs. Tj (from LINx to LOx)
Figure 15-13	Minimum transmittable pulse width for high-side switching, $tHIN_{(MIN)}$ vs. Tj
Figure 15-14	Minimum transmittable pulse width for low-side switching, $tLIN_{(MIN)}$ vs. Tj
Figure 15-15	Typical output pulse widths, tHO, tLO vs. input pulse widths, tHIN, tLIN
Figure 15-16	FOx Pin Voltage in Normal Operation, VFOL vs. Tj
Figure 15-17	Logic Operation Start Voltage, $VBS_{(ON)}$ vs. Tj
Figure 15-18	Logic Operation Stop Voltage, $VBS_{(OFF)}$ vs. Tj
Figure 15-19	Logic Operation Start Voltage, $VCC_{(ON)}$ vs. Tj
Figure 15-20	Logic Operation Stop Voltage, $VCC_{(OFF)}$ vs. Tj
Figure 15-21	UVLO_VB filtering time vs. Tj
Figure 15-22	UVLO_VCC filtering time vs. Tj
Figure 15-23	Overcurrent Protection Threshold Voltage, VTRIP vs. Tj
Figure 15-24	Blanking Time, tBK + propagation delay, tD vs. Tj
Figure 15-25	Overcurrent Protection Hold Time, tP vs. Tj
Figure 15-26	Filtering time of Simultaneous On-state Prevention Function vs. Tj

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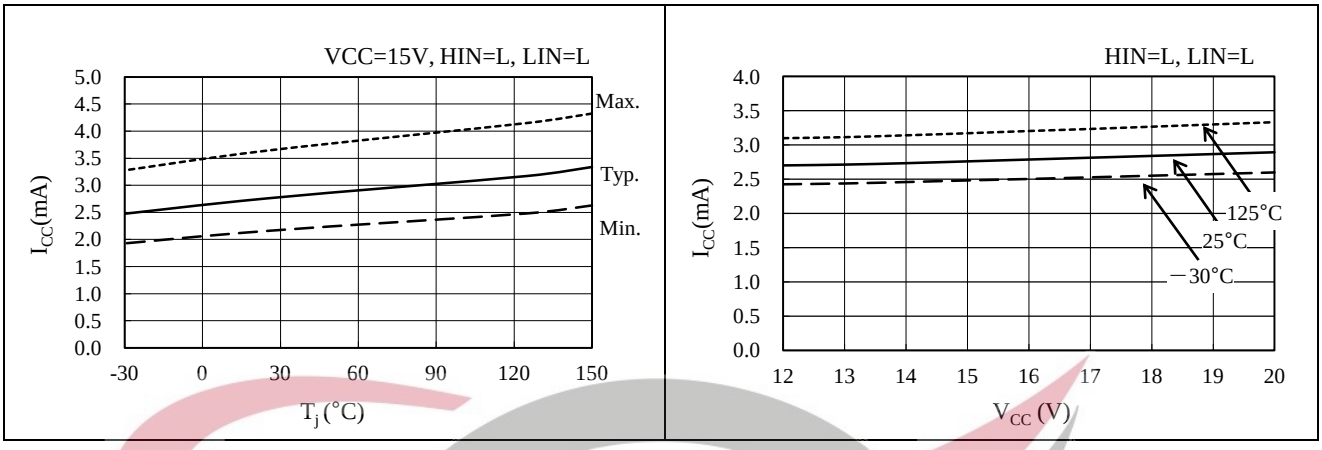

Figure 15-1. Logic Supply Current in three-phase operating, I_{CC} vs. T_j

Figure 15-2. Logic Supply Current in three-phase operating, I_{CC} vs. VCCx pin voltage, V_{CC}

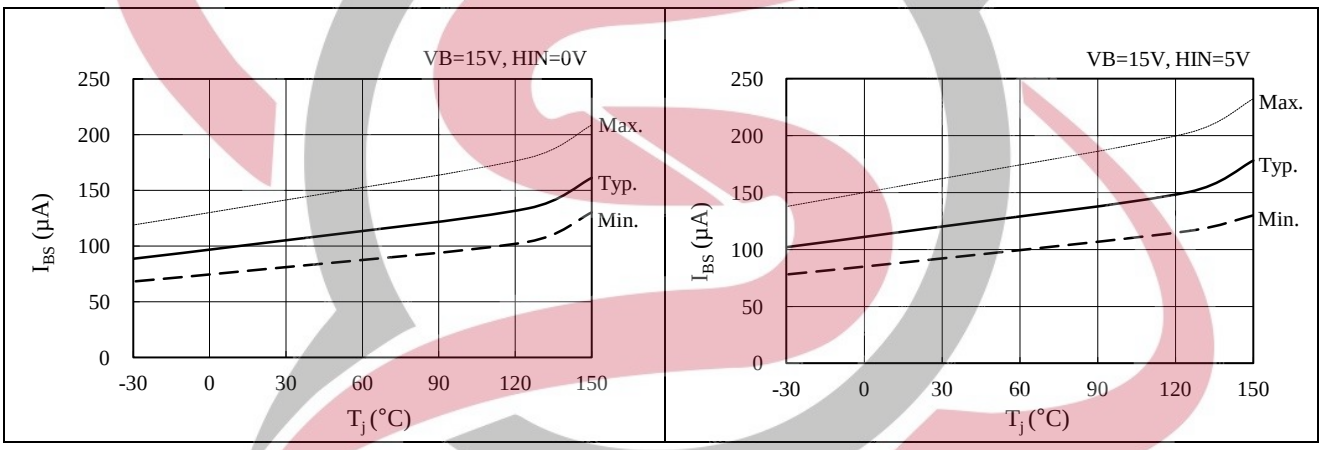

Figure 15-3. Logic Supply Current in single-phase operating (HINx = 0 V), I_{BS} vs. T_j

Figure 15-4. Logic Supply Current in single-phase operating (HINx = 5 V), I_{BS} vs. T_j

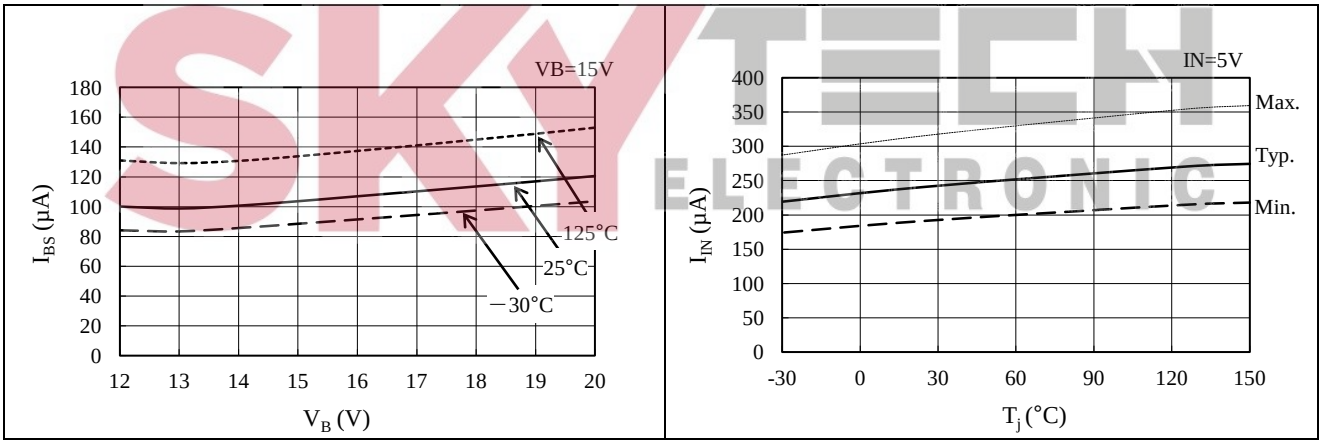

Figure 15-5. Logic Supply Current in single-phase operating (HINx = 0 V), I_{BS} vs. VBx pin voltage, V_B

Figure 15-6. Input Current at High Level (HINx or LINx) vs. T_j

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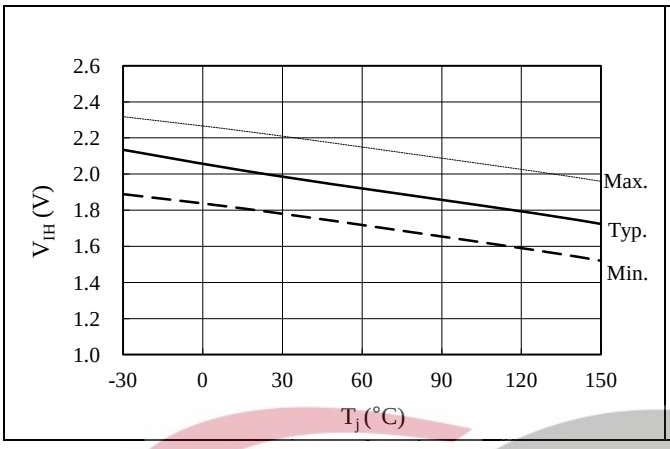

Figure 15-7. High Level Input Signal Threshold Voltage, V_{IH} vs. T_j

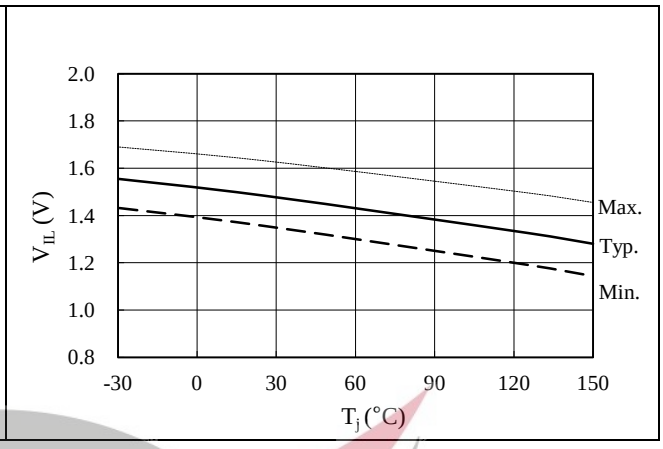

Figure 15-8. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_j

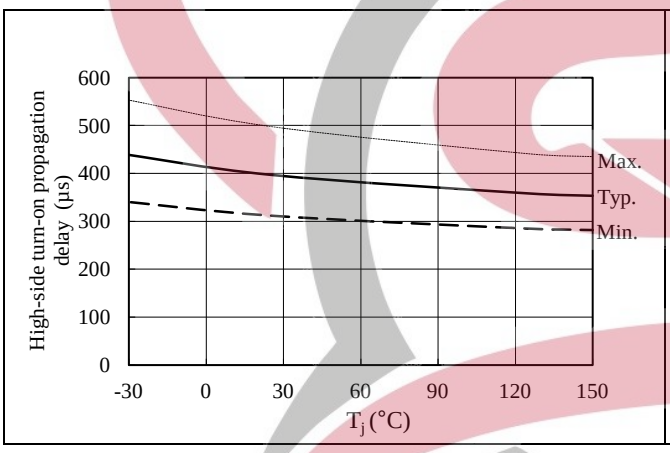

Figure 15-9. High-side turn-on propagation delay vs. T_j (from HINx to HOx)

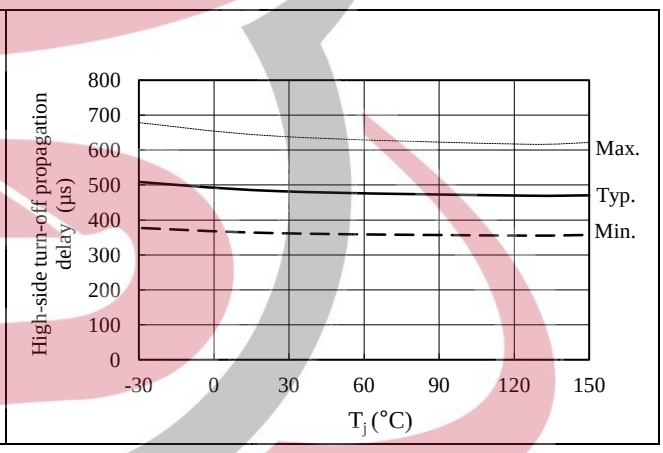

Figure 15-10. High-side turn-off propagation delay vs. T_j (from HINx to HOx)

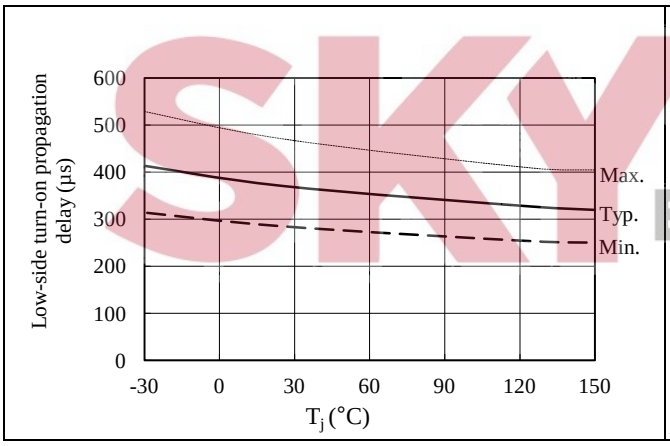

Figure 15-11. Low-side turn-on propagation delay vs. T_j (from LINx to LOx)

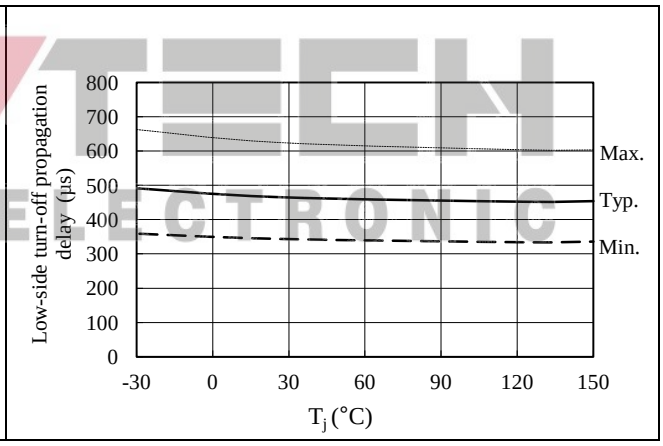

Figure 15-12. Low-side turn-off propagation delay vs. T_j (from LINx to LOx)

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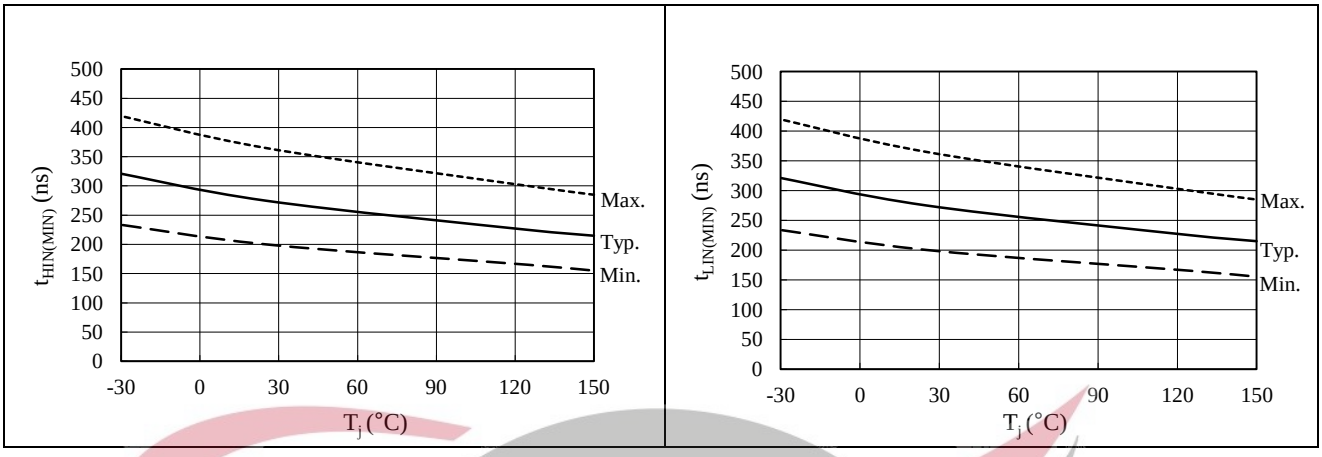

Figure 15-13. Minimum transmittable pulse width for high-side switching, $t_{HIN(MIN)}$ vs. T_j

Figure 15-14. Minimum transmittable pulse width for low-side switching, $t_{LIN(MIN)}$ vs. T_j

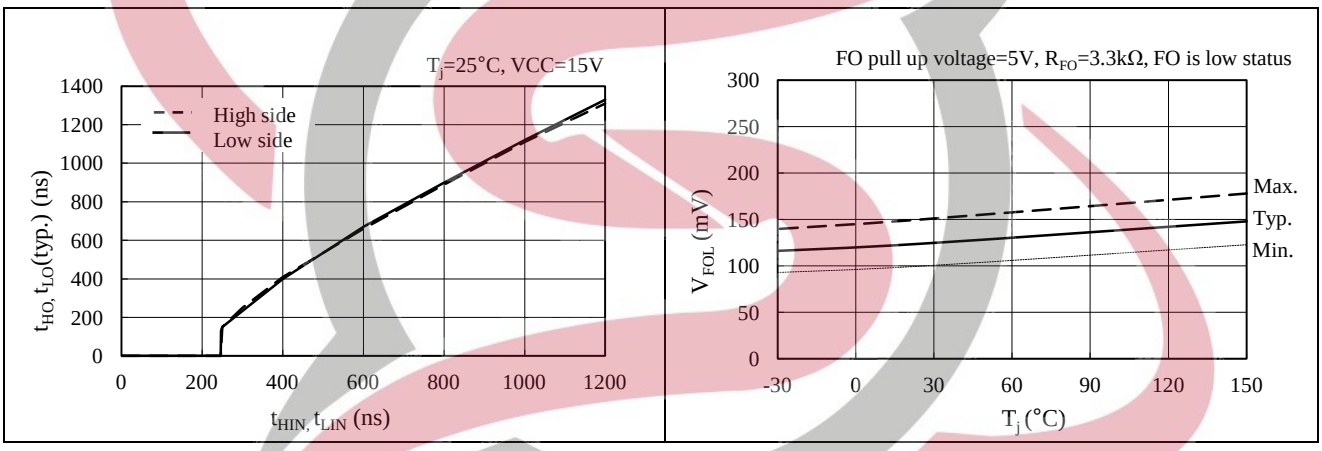

Figure 15-15. Typical output pulse widths, t_{HO}, t_{LO} vs. input pulse widths, t_{HIN}, t_{LIN}

Figure 15-16. FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_j

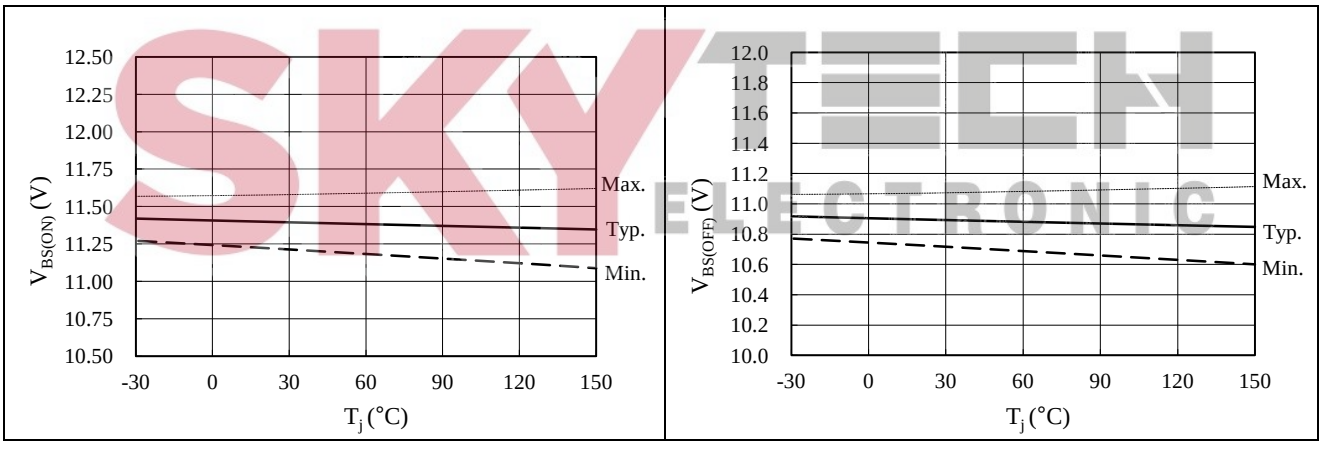

Figure 15-17. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_j

Figure 15-18. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_j

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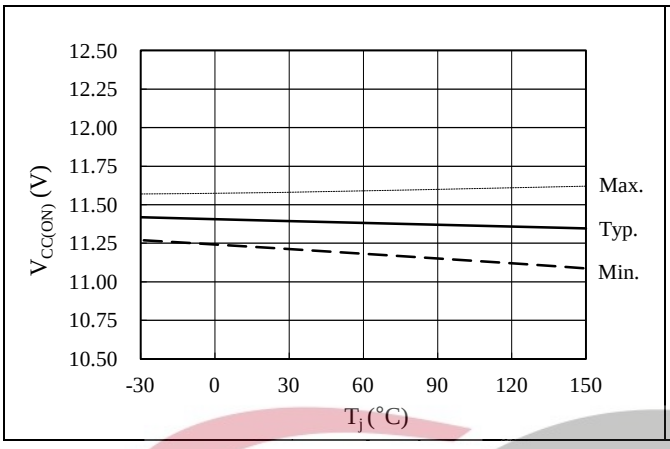

Figure 15-19. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_j

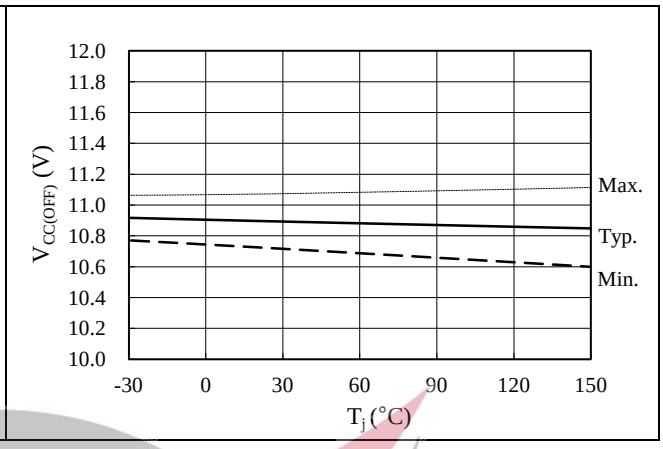

Figure 15-20. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_j

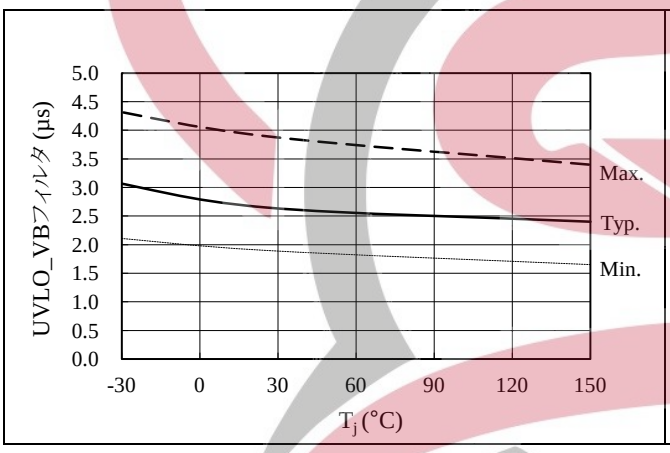

Figure 15-21. UVLO_VB filtering time vs. T_j

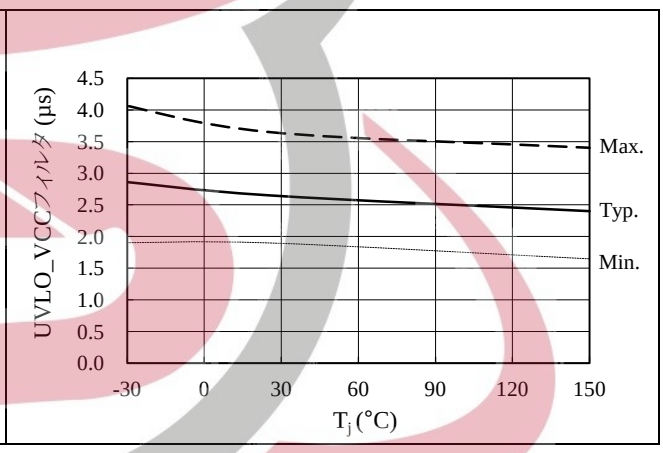

Figure 15-22. UVLO_VCC filtering time vs. T_j

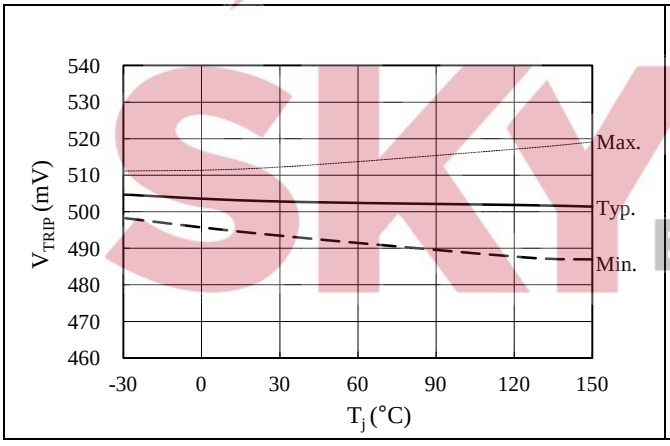

Figure 15-23. Overcurrent Protection Threshold Voltage, V_{TRIP} vs. T_j

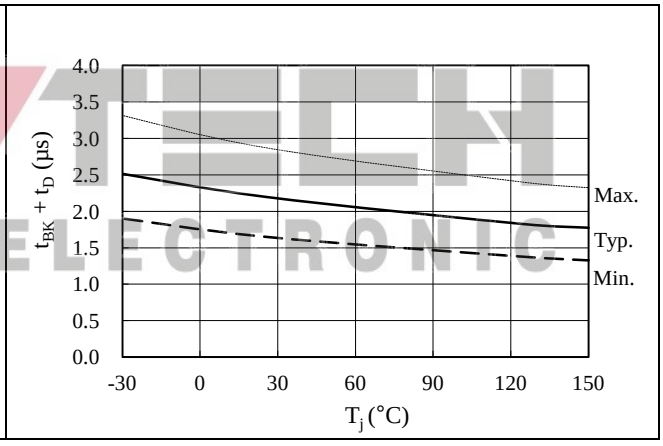

Figure 15-24. Blanking Time, t_{BK} + propagation delay, t_D vs. T_j

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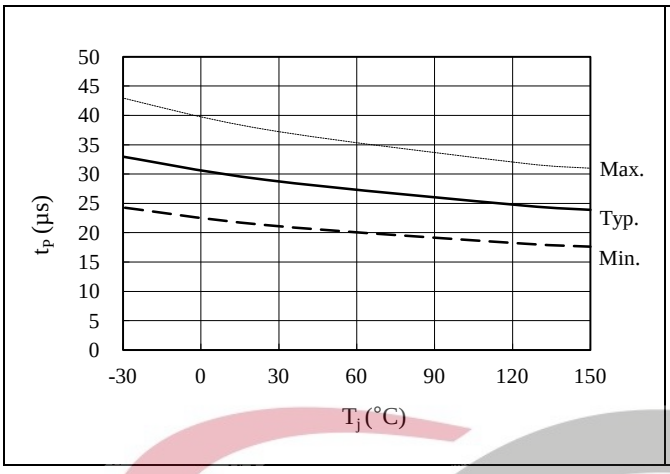

Figure 15-25. Overcurrent Protection Hold Time, t_p vs. T_j

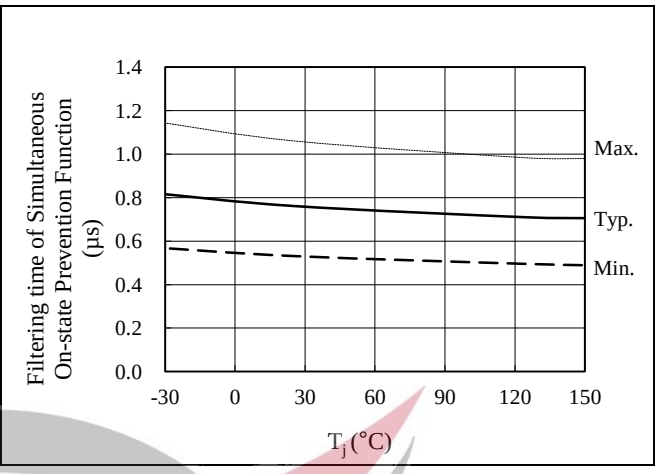

Figure 15-26. Filtering time of Simultaneous On-state Prevention Function vs. T_j

15.3. Performance Curves of Output Parts

15.3.1. Output Transistor Performance Curves

15.3.1.1. SCM1261M

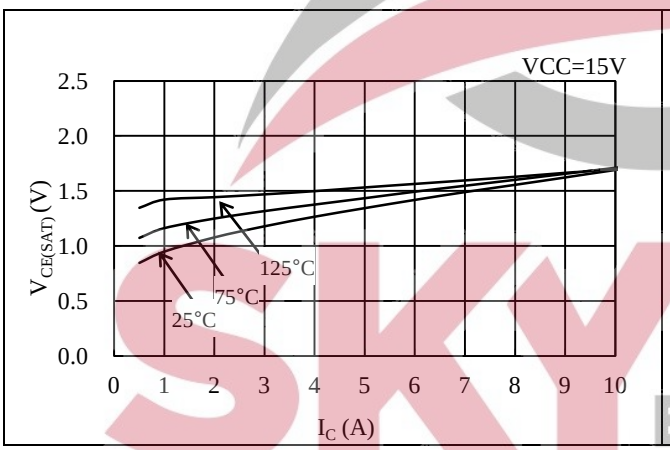

Figure 15-27. IGBT $V_{CE(SAT)}$ vs. I_C

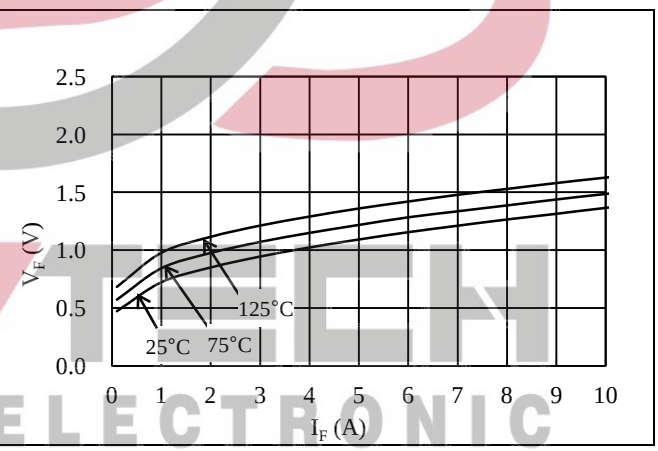

Figure 15-28. Freewheeling diode V_F vs. I_F

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15.3.1.2. SCM1242MF, SCM1263MF, SCM1243MF

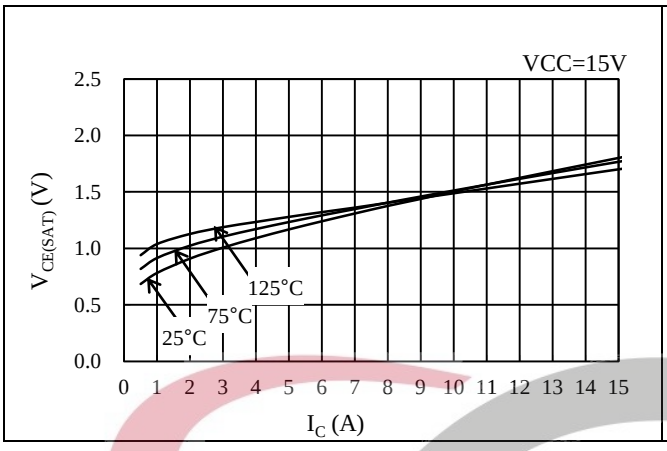

Figure 15-29. IGBT $V_{CE(SAT)}$ vs. I_C

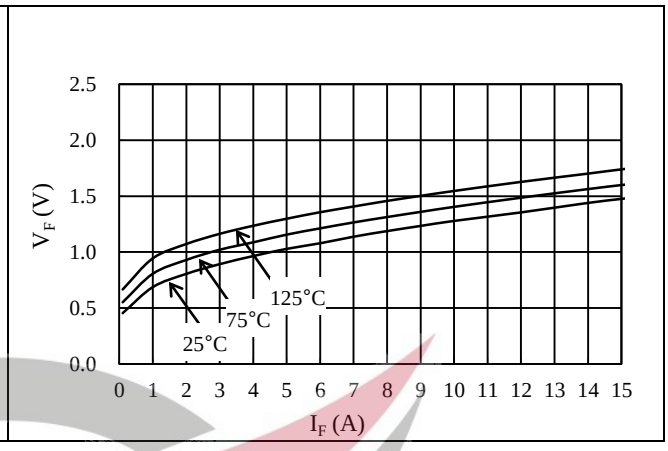

Figure 15-30. Freewheeling diode V_F vs. I_F

15.3.1.3. SCM1265MF, SCM1245MF

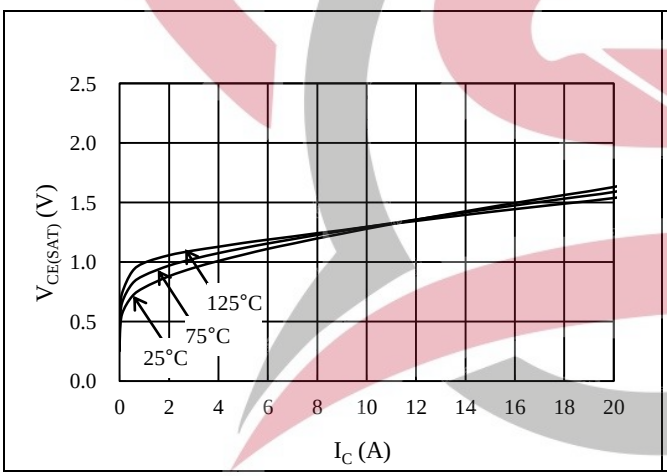

Figure 15-31. IGBT $V_{CE(SAT)}$ vs. I_C

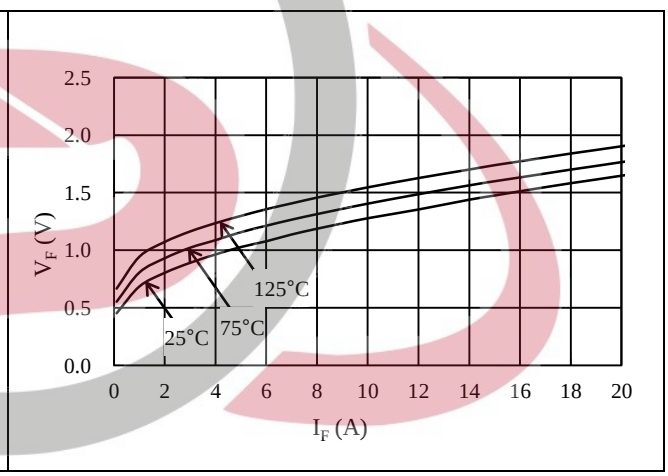

Figure 15-32. Freewheeling diode V_F vs. I_F

15.3.1.4. SCM1256MF, SCM1246MF

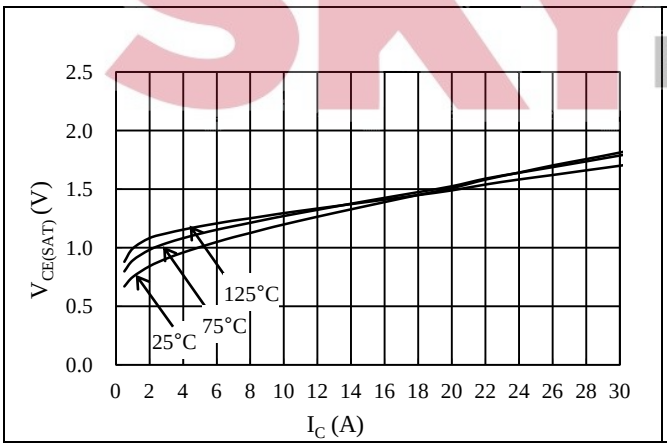

Figure 15-33. IGBT $V_{CE(SAT)}$ vs. I_C

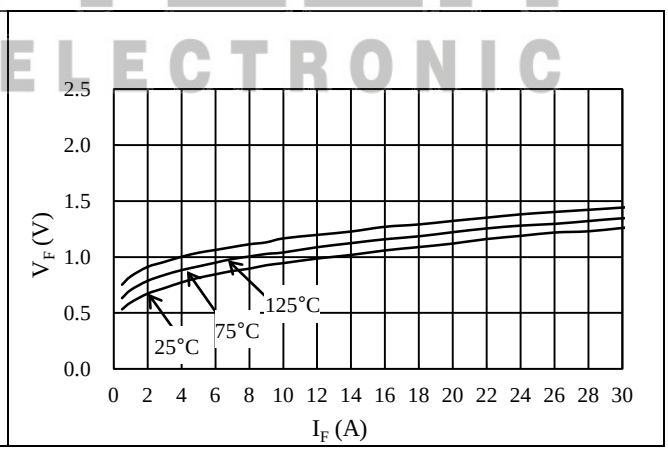

Figure 15-34. Freewheeling diode V_F vs. I_F

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15.3.2. Switching Loss

Conditions: VBB = 300 V, half-bridge circuit with inductance load.

15.3.2.1. SCM1261MF

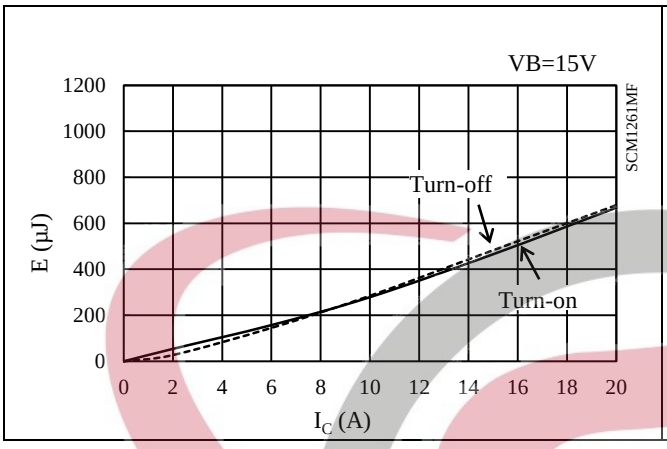

Figure 15-35. High-side switching loss (T_j = 25°C)

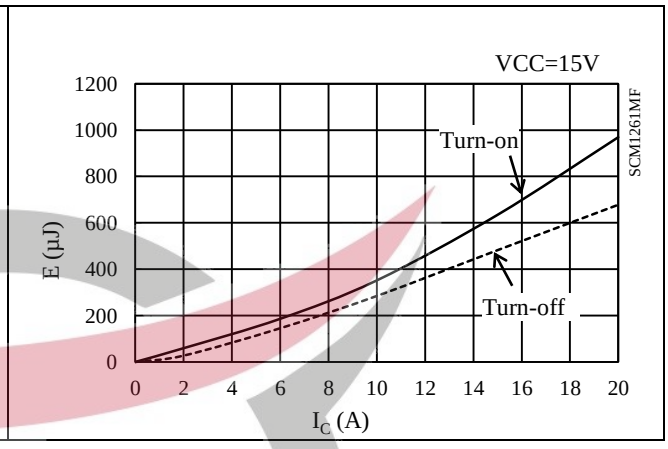

Figure 15-36. Low-side switching loss (T_j = 25°C)

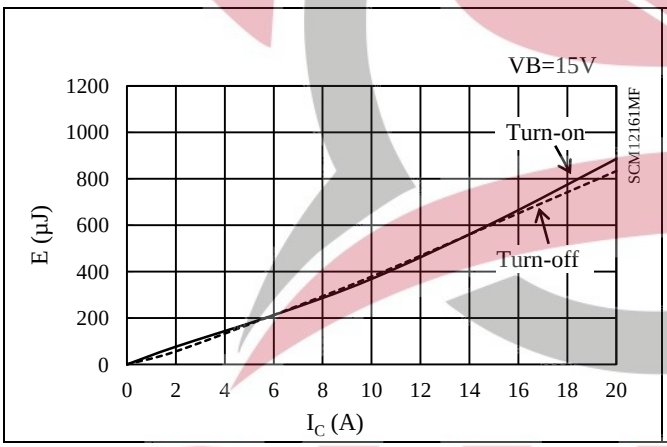

Figure 15-37. High-side switching loss (T_j = 125°C)

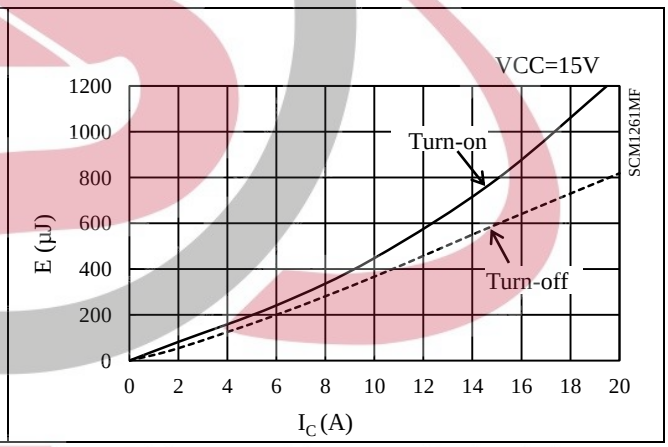

Figure 15-38. Low-side switching loss (T_j = 125°C)

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15.3.2.2. SCM1242MF

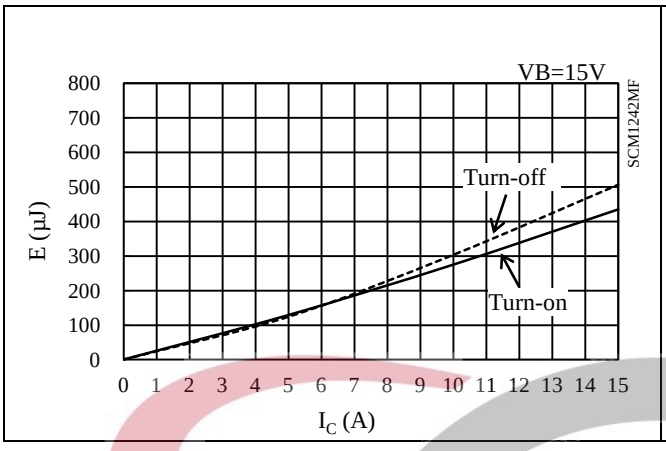

Figure 15-39 High-side switching loss (T_j = 25°C)

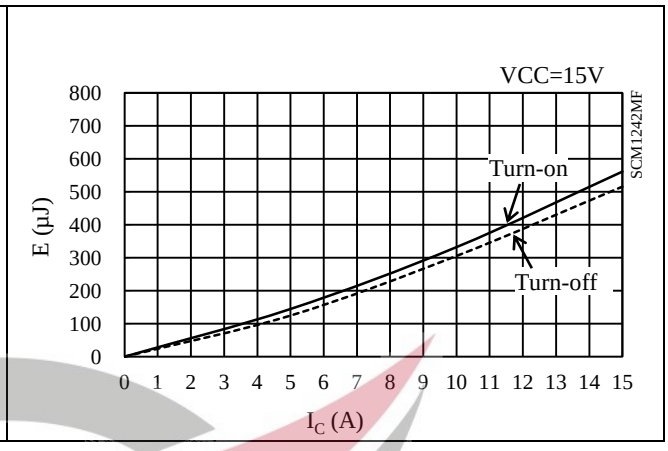

Figure 15-40. Low-side switching loss (T_j = 25°C)

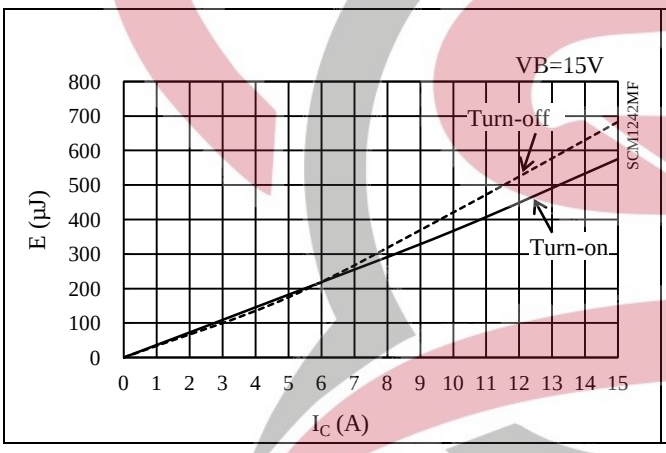

Figure 15-41. High-side switching loss (T_j = 125°C)

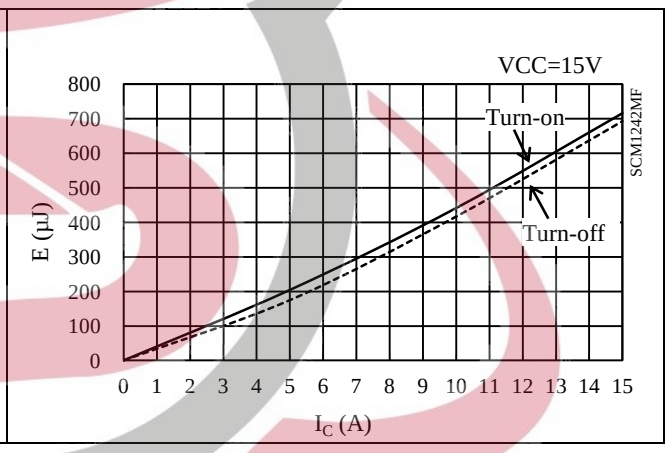

Figure 15-42. Low-side switching loss (T_j = 125°C)

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15.3.2.3. SCM1263MF

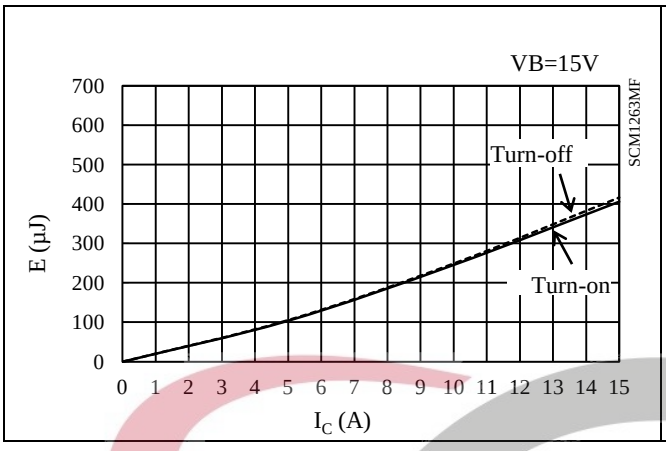

Figure 15-43 High-side switching loss (T_j = 25°C)

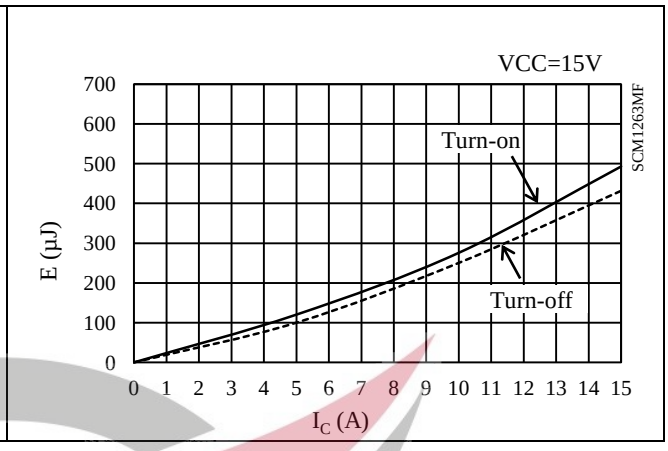

Figure 15-44. Low-side switching loss (T_j = 25°C)

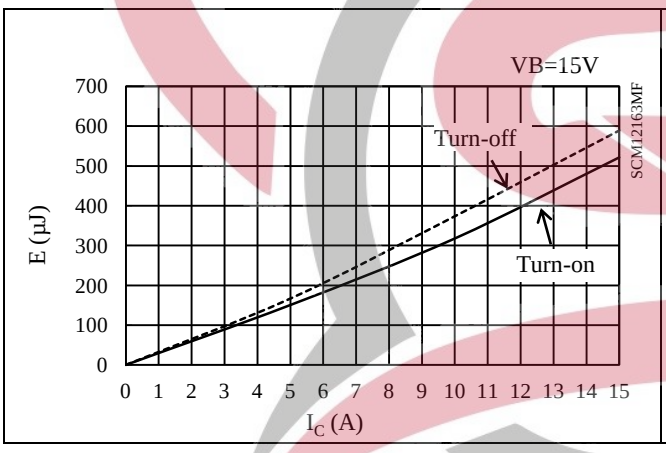

Figure 15-45. High-side switching loss (T_j = 125°C)

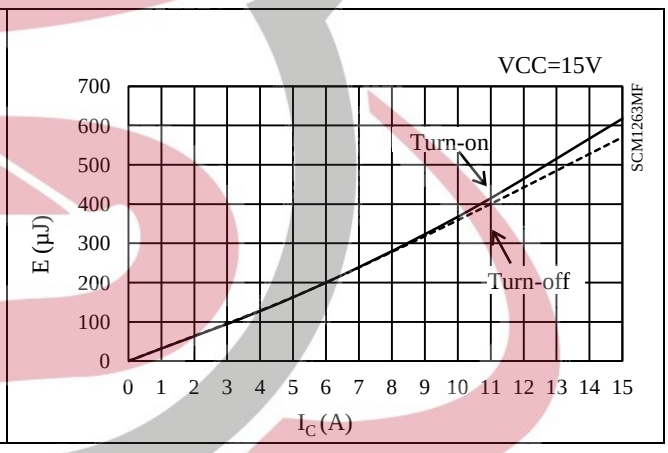

Figure 15-46. Low-side switching loss (T_j = 125°C)

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15.3.2.4. SCM1243MF

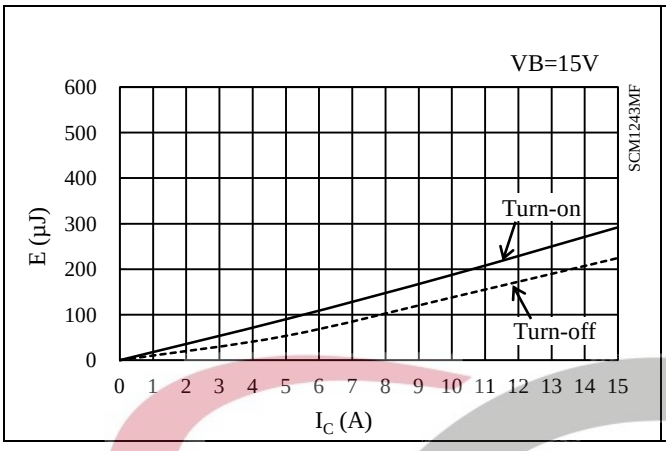

Figure 15-47 High-side switching loss (T_j = 25°C)

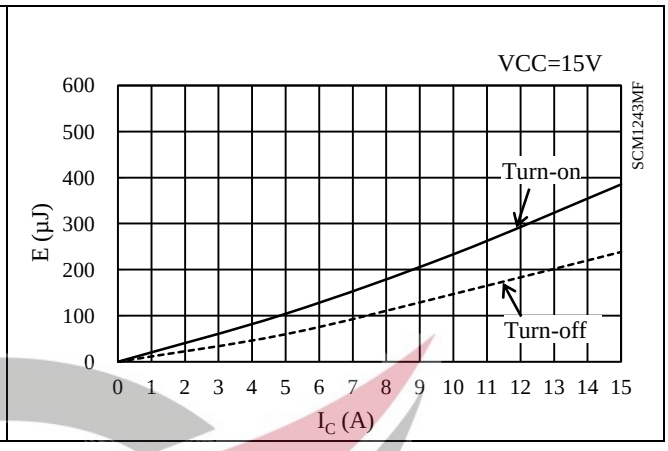

Figure 15-48. Low-side switching loss (T_j = 25°C)

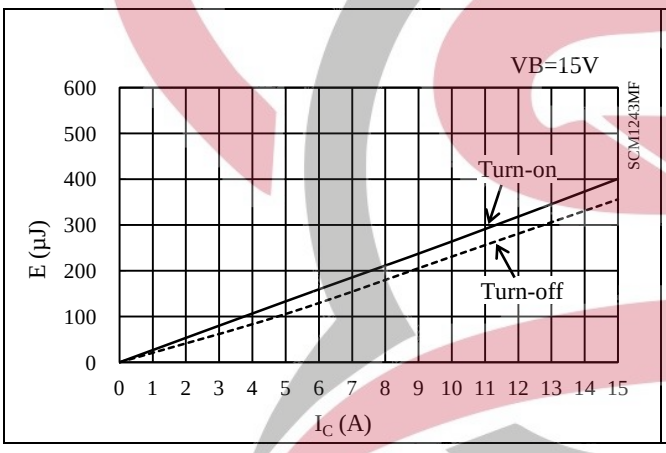

Figure 15-49. High-side switching loss (T_j = 125°C)

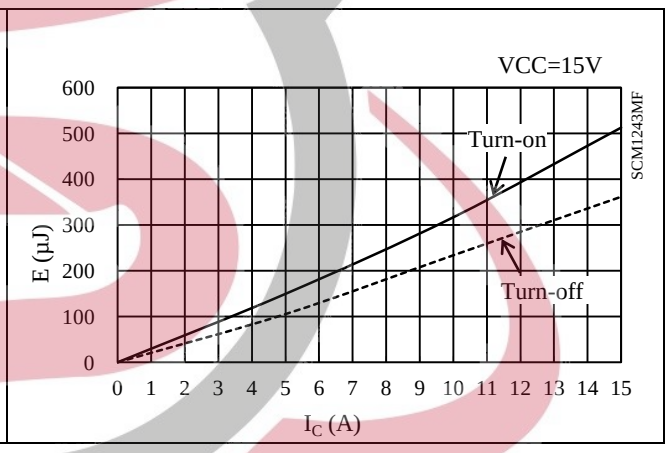

Figure 15-50. Low-side switching loss (T_j = 125°C)

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15.3.2.5. SCM1265MF

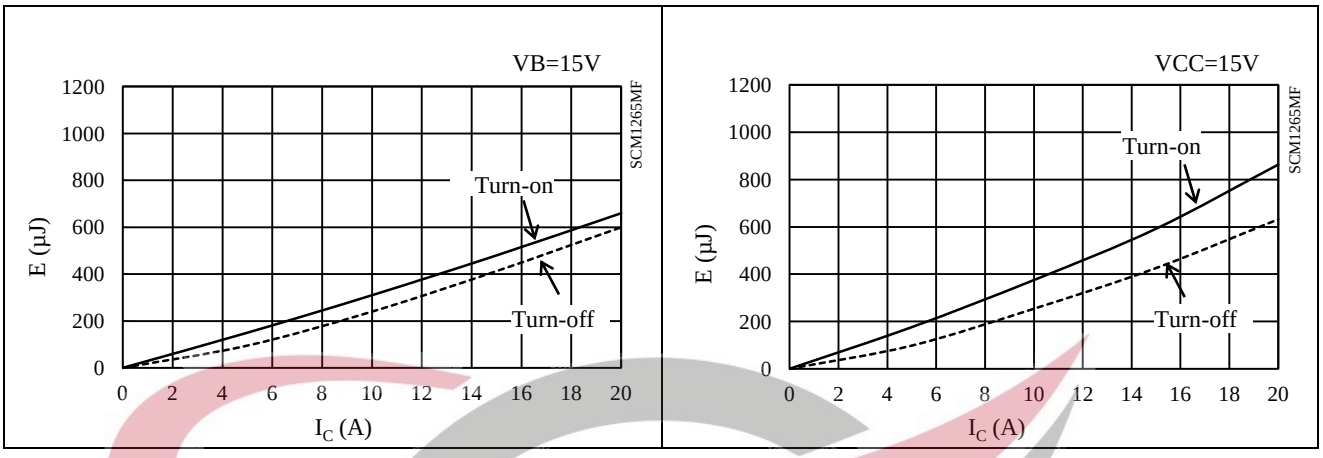

Figure 15-51 High-side switching loss (T_j = 25°C)

Figure 15-52. Low-side switching loss (T_j = 25°C)

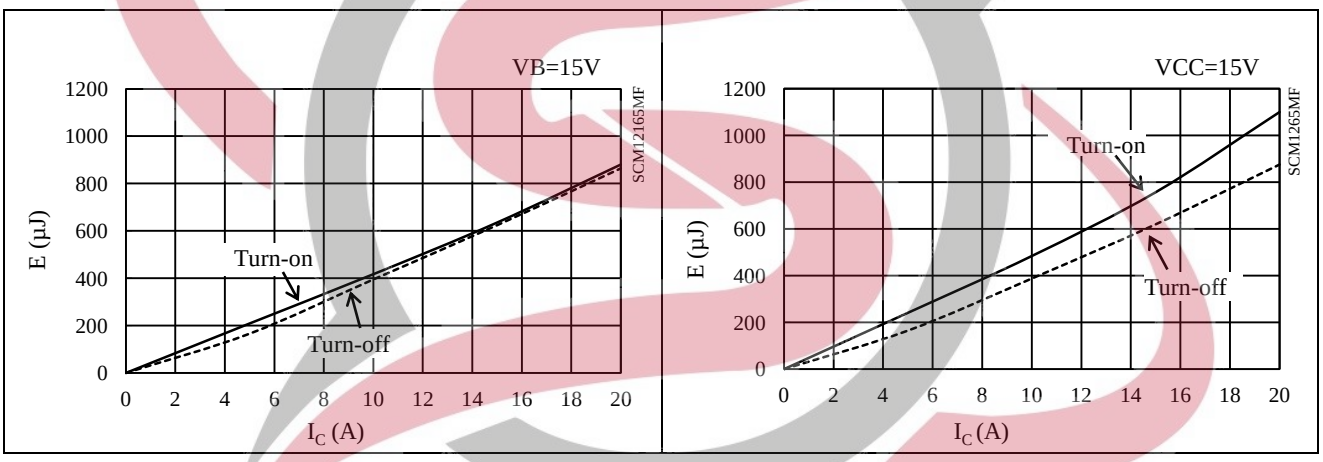

Figure 15-53. High-side switching loss (T_j = 125°C)

Figure 15-54. Low-side switching loss (T_j = 125°C)

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15.3.2.6. SCM1245MF

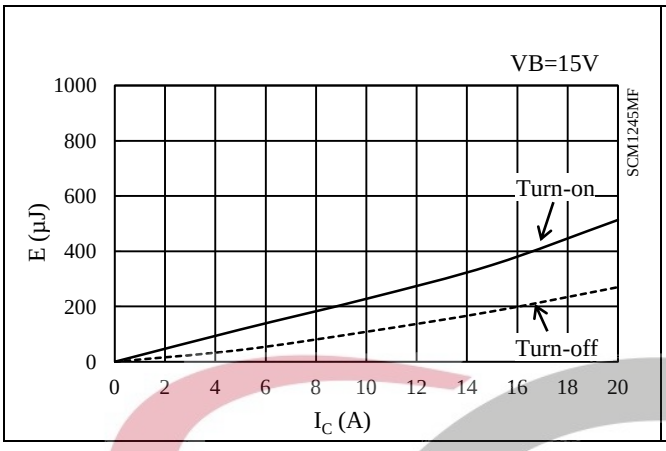

Figure 15-55 High-side switching loss (T_j = 25°C)

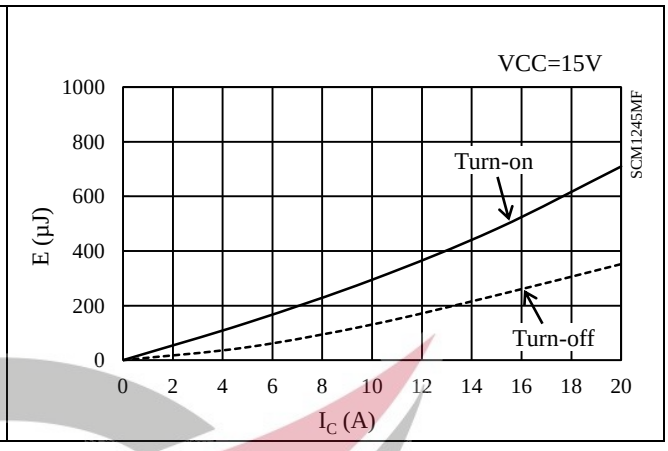

Figure 15-56. Low-side switching loss (T_j = 25°C)

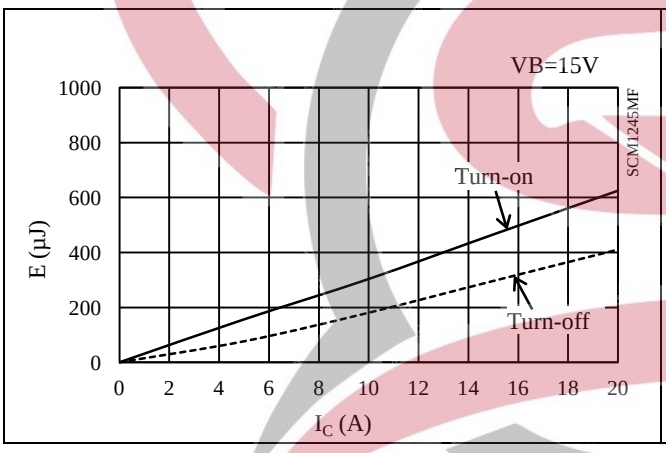

Figure 15-57. High-side switching loss (T_j = 125°C)

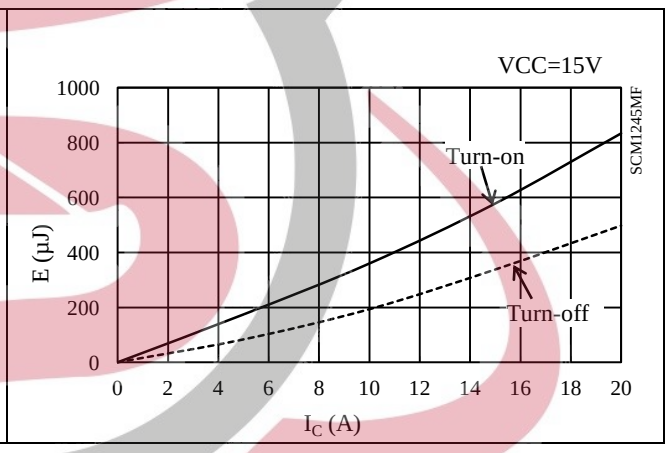

Figure 15-58. Low-side switching loss (T_j = 125°C)

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15.3.2.7. SCM1256MF

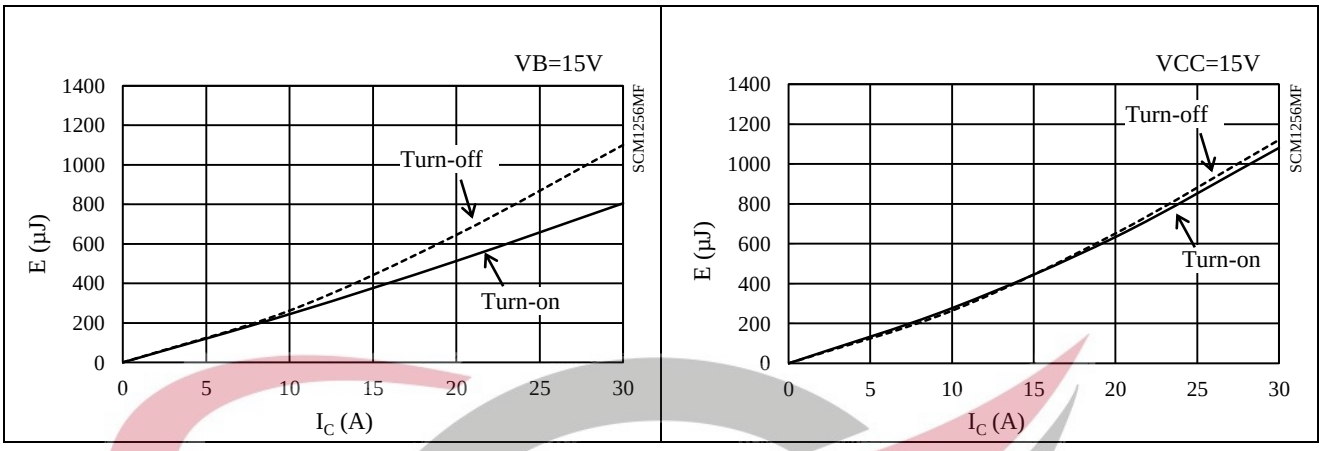

Figure 15-59 High-side switching loss (T_j = 25°C)

Figure 15-60. Low-side switching loss (T_j = 25°C)

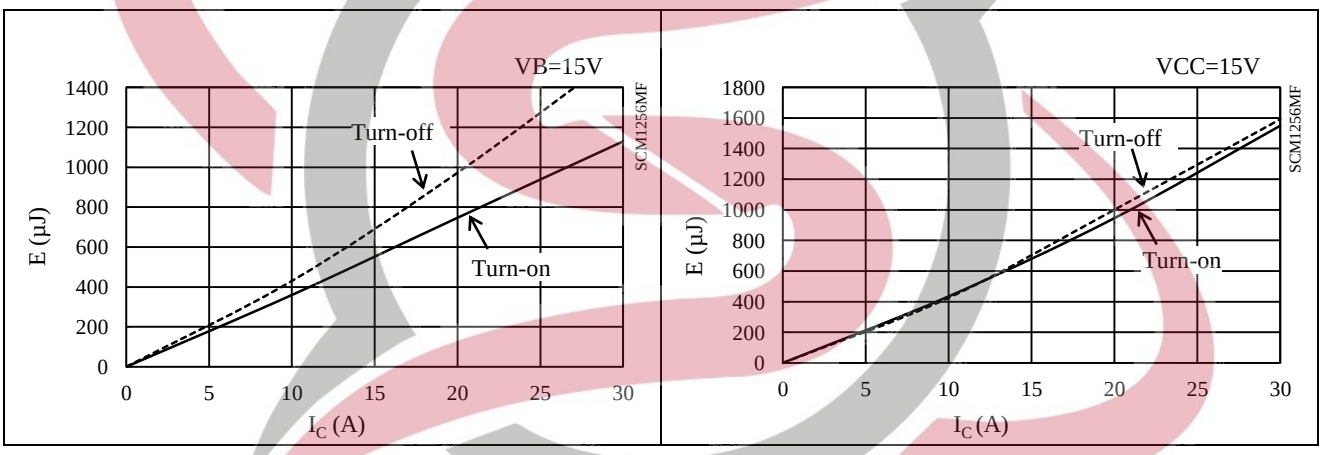

Figure 15-61. High-side switching loss (T_j = 125°C)

Figure 15-62. Low-side switching loss (T_j = 125°C)

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15.3.2.8. SCM1246MF

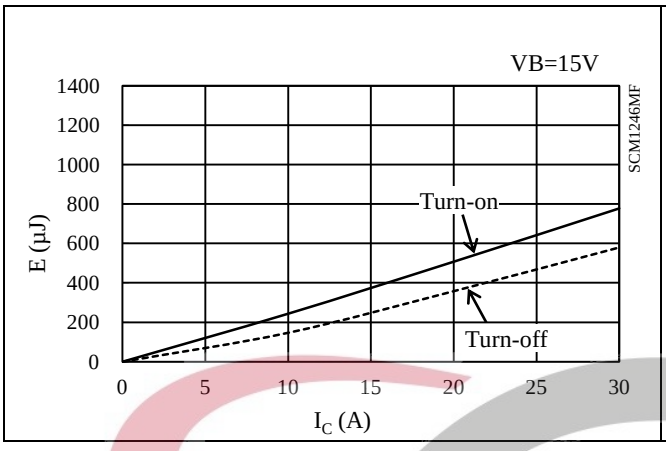

Figure 15-63 High-side switching loss (T_j = 25°C)

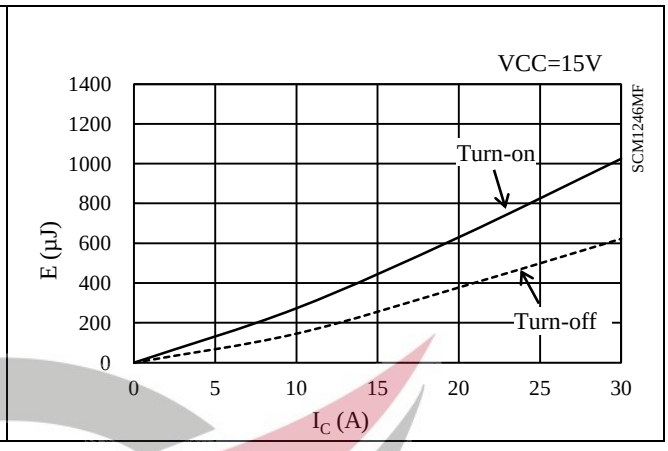

Figure 15-64. Low-side switching loss (T_j = 25°C)

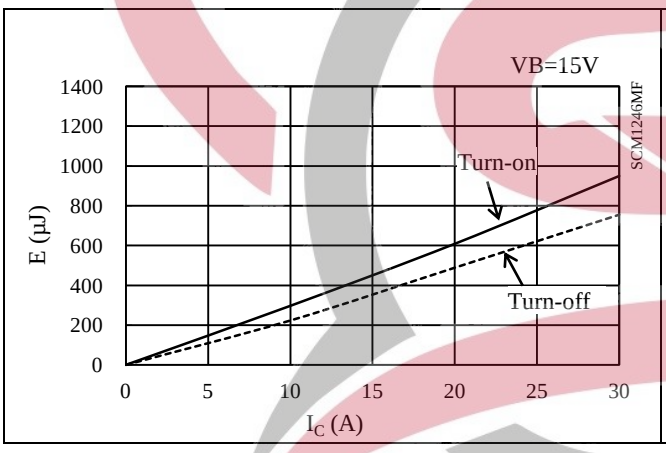

Figure 15-65. High-side switching loss (T_j = 125°C)

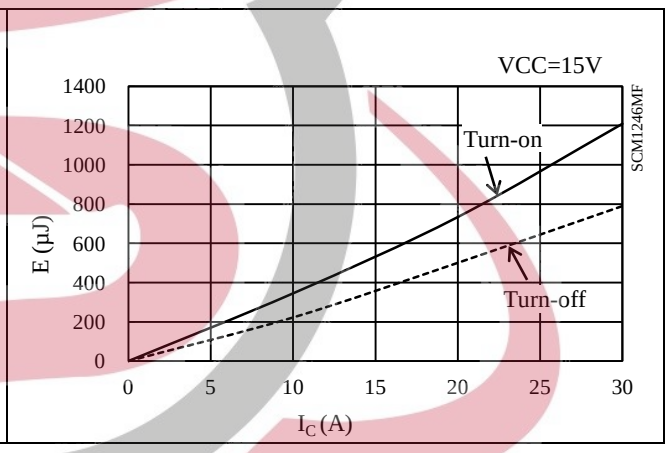

Figure 15-66. Low-side switching loss (T_j = 125°C)

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15.4. Allowable Effective Current Curves

The following curves represent allowable effective currents in sine-wave driving under a three-phase PWM system. All the values listed in this section, including $V_{CE(SAT)}$ of output transistors and switching losses, are typical values.

Operating conditions: VBB pin input voltage (V_{DC}) = 300 V, VCCx pin input voltage (V_{CC}) = 15 V, modulation index (M) = 0.9, motor power factor (cosθ) = 0.8, junction temperature (T_j) = 150°C.

15.4.1. SCM1261MF

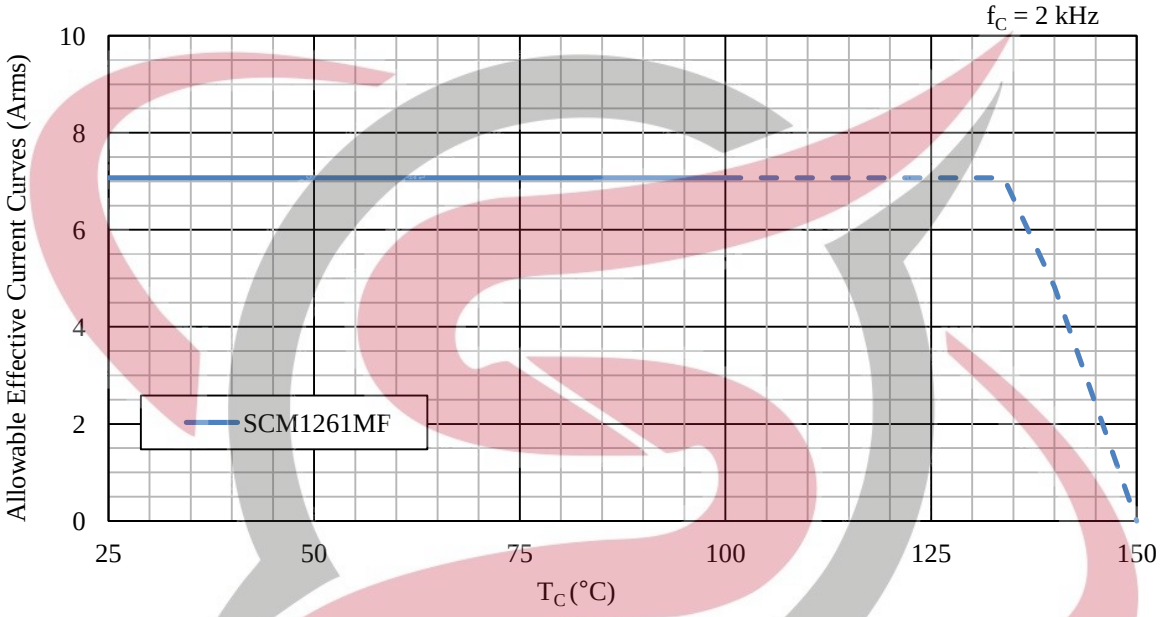

Figure 15-67. Allowable effective current, 10 A device (f_C = 2 kHz)

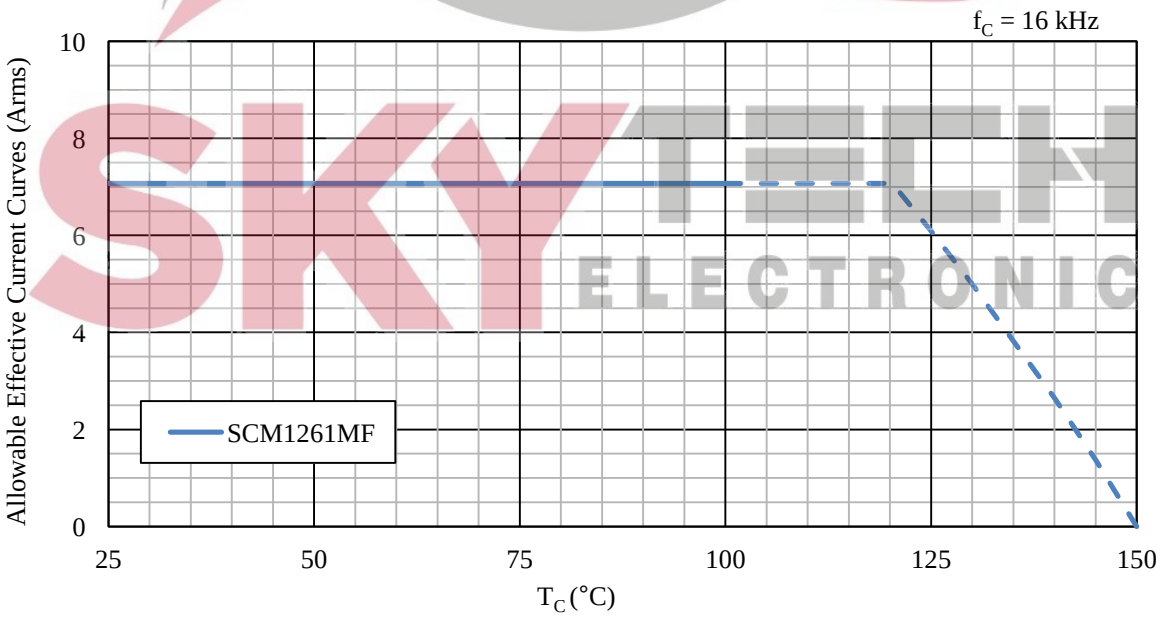

Figure 15-68. Allowable effective current, 10 A device (f_C = 16 kHz)

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15.4.2. SCM1242MF, SCM1263MF, SCM1243MF

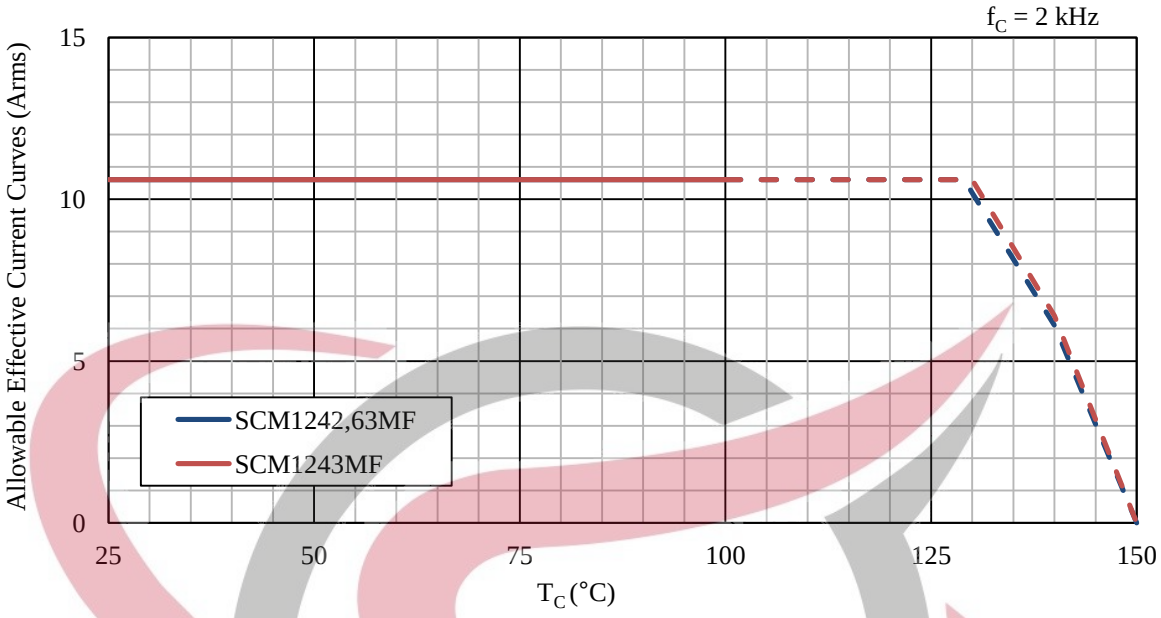

Figure 15-69. Allowable effective current, 15 A device (f_C = 2 kHz)

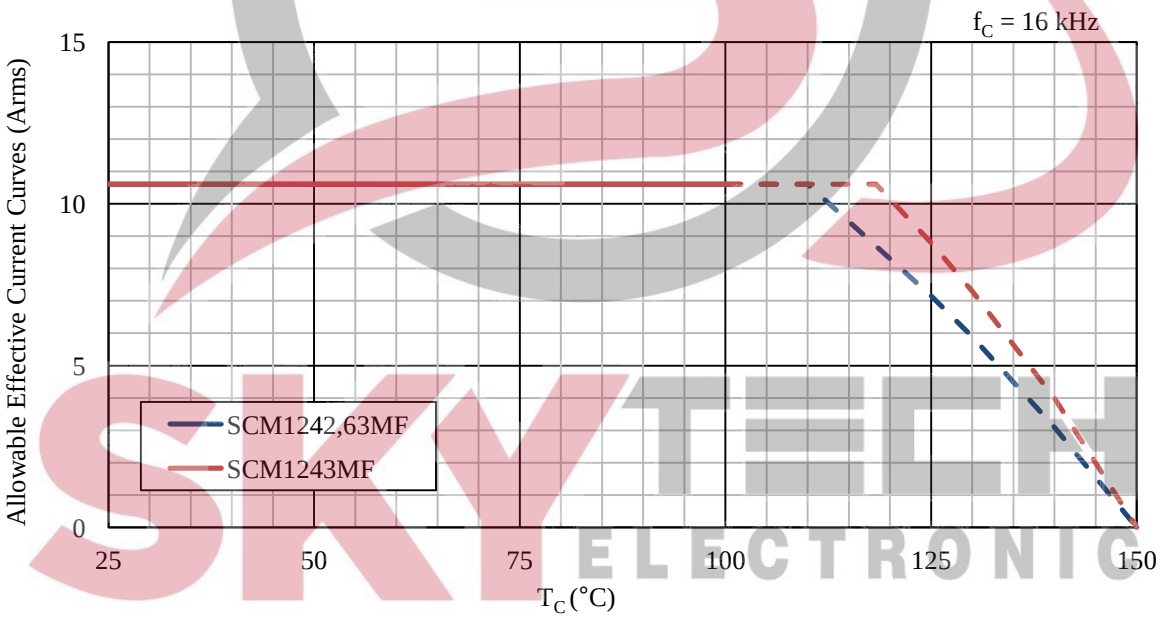

Figure 15-70. Allowable effective current, 15 A device (f_C = 16 kHz)

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15.4.3. SCM1265MF, SCM1245MF

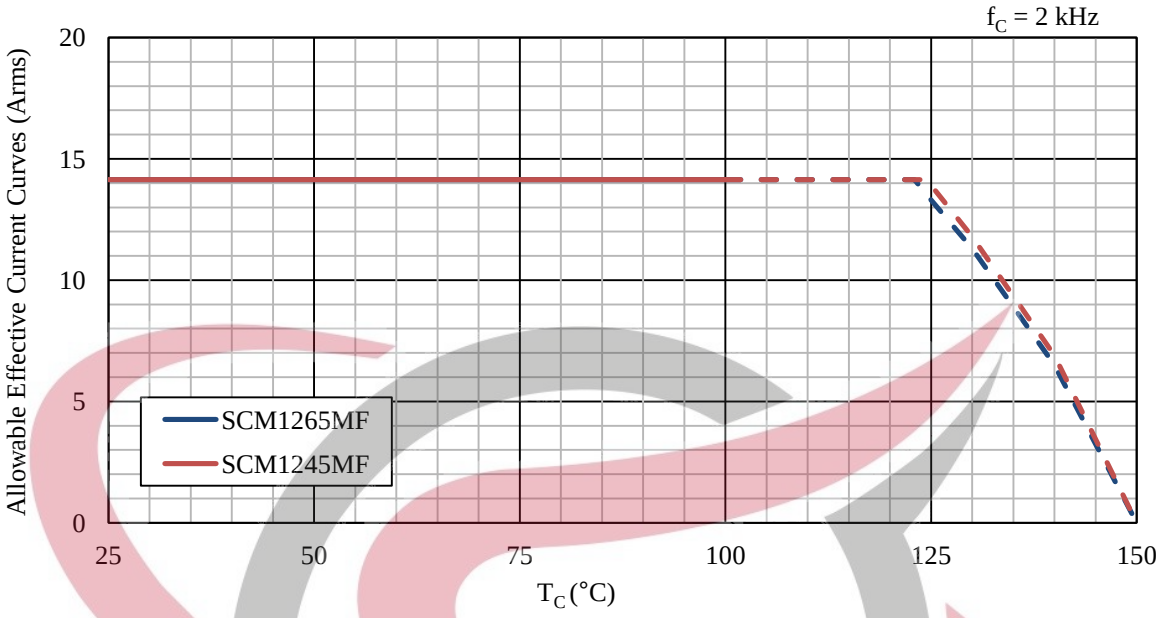

Figure 15-71. Allowable effective current, 20 A device (f_C = 2 kHz)

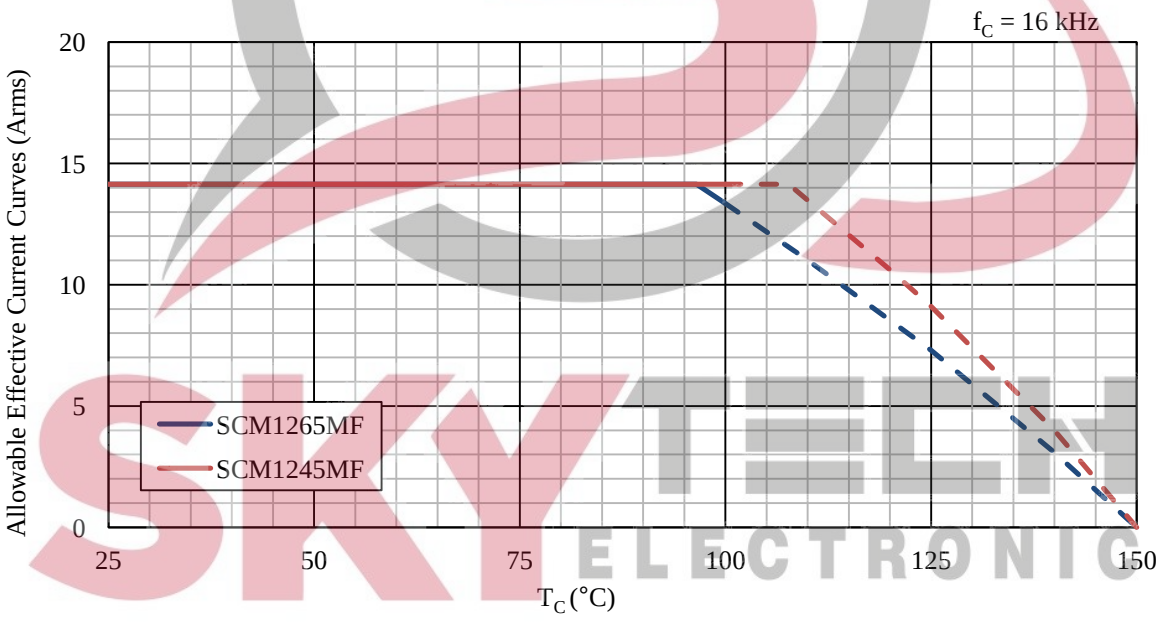

Figure 15-72. Allowable effective current, 20 A device (f_C = 16 kHz)

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15.4.4. SCM1256MF, SCM1246MF

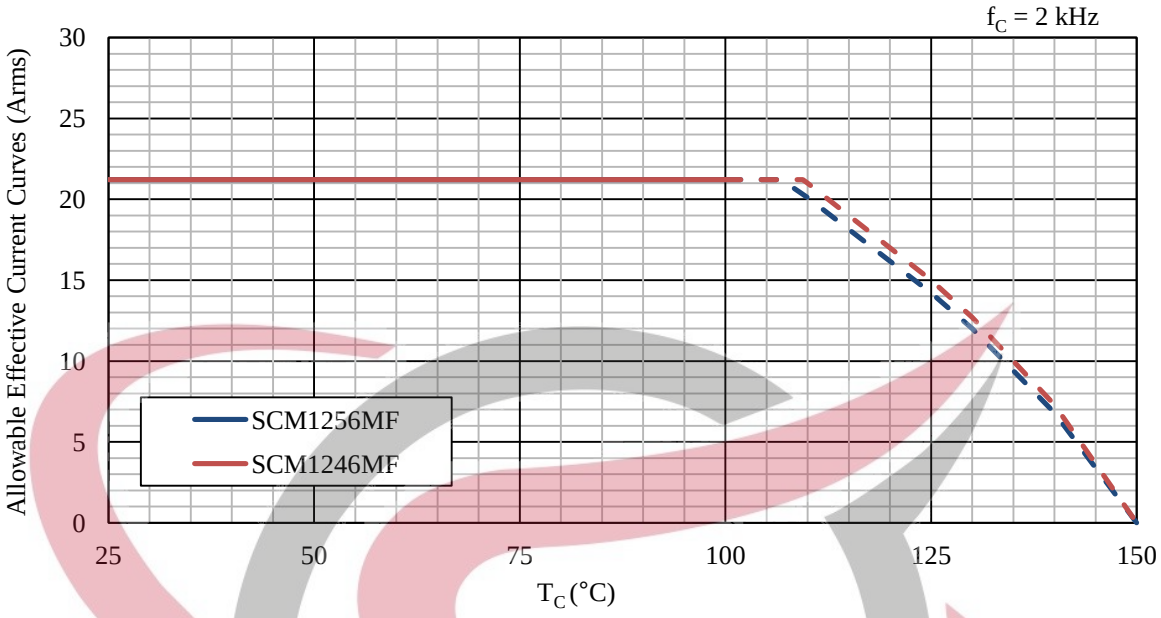

Figure 15-73. Allowable effective current, 30 A device (f_C = 2 kHz)

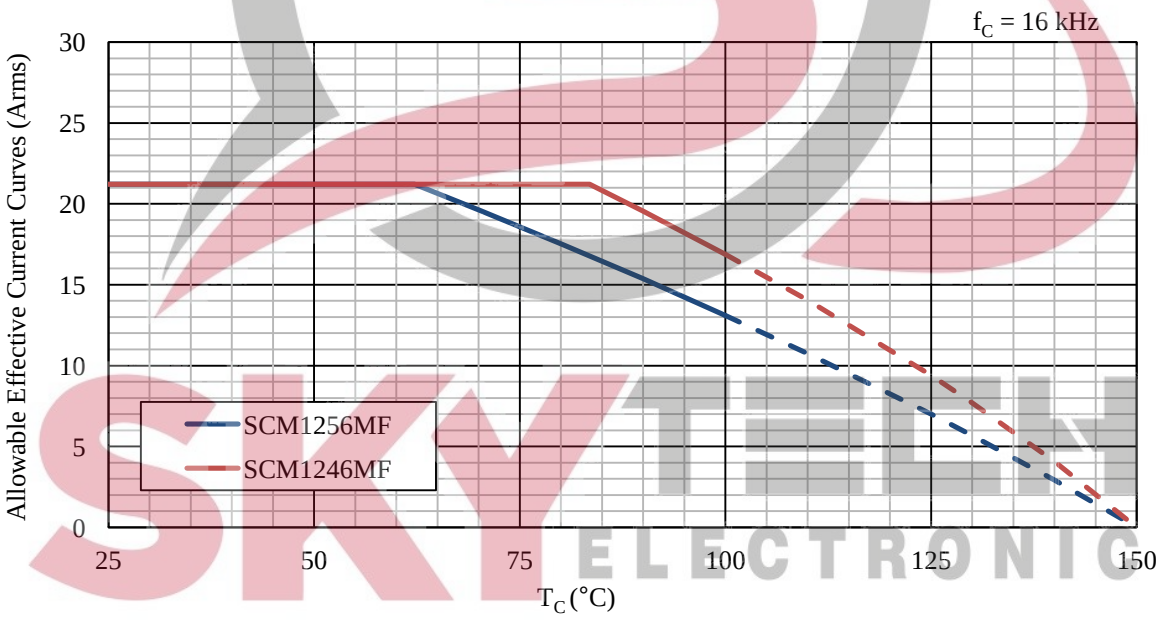

Figure 15-74. Allowable effective current, 30 A device (f_C = 16 kHz)

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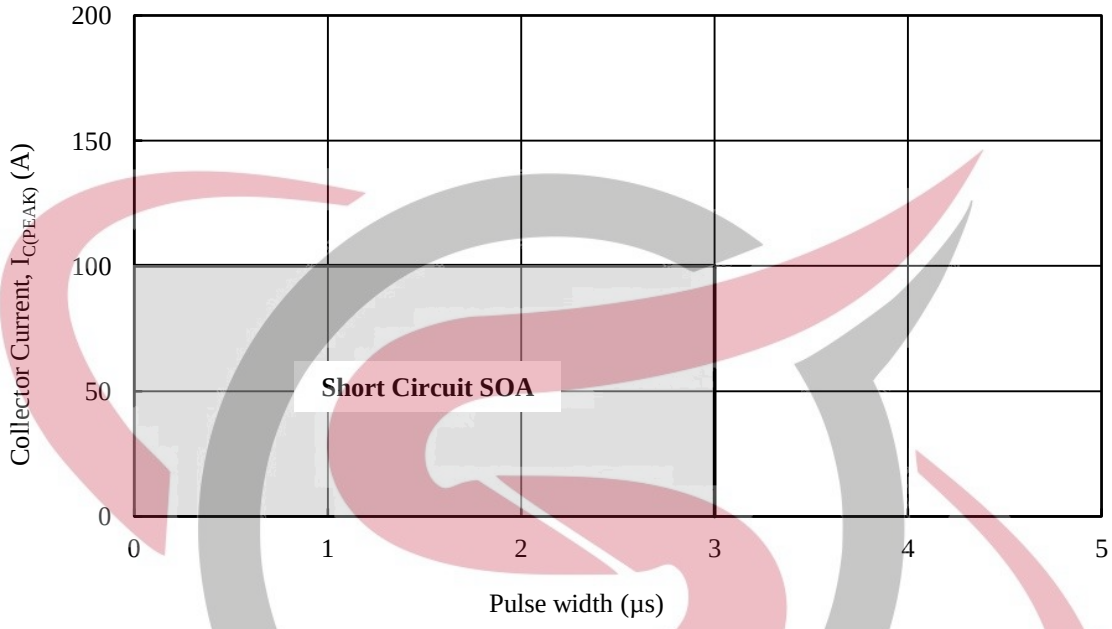
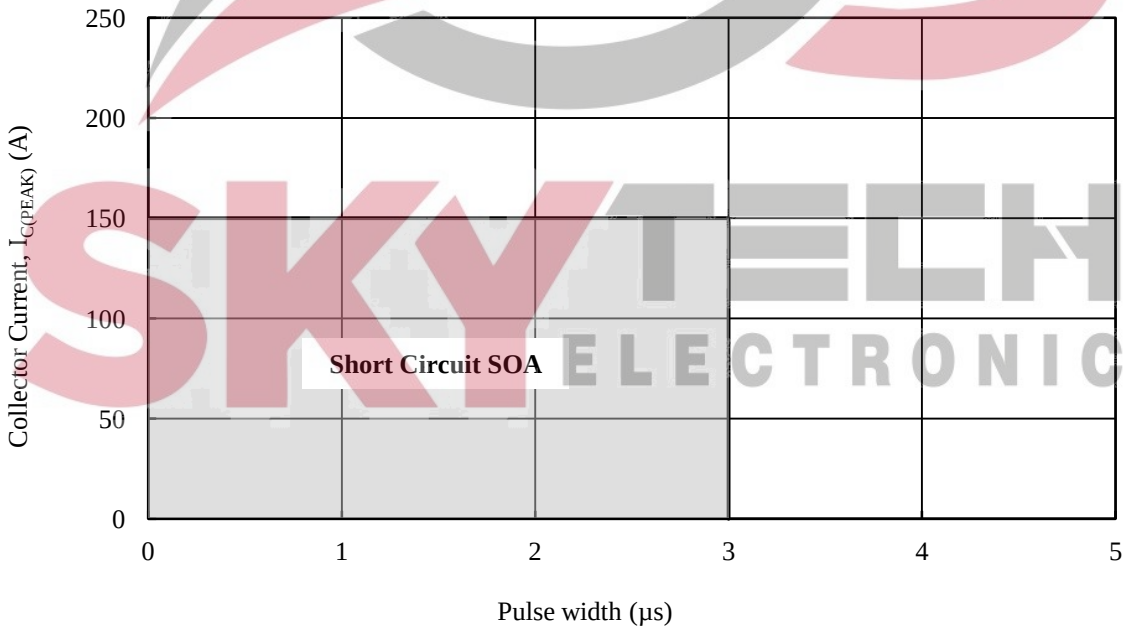
15.5. Short Circuit SOA (Safe Operating Area)

Conditions: $V_{DC} \leq 400$ V, $13.5\ V \leq V_{CC} \leq 16.5$ V, $T_j = 125°C$, 1 pulse.

15.5.1. SCM1261MF



15.5.2. SCM1242MF, SCM1263MF, SCM1243MF



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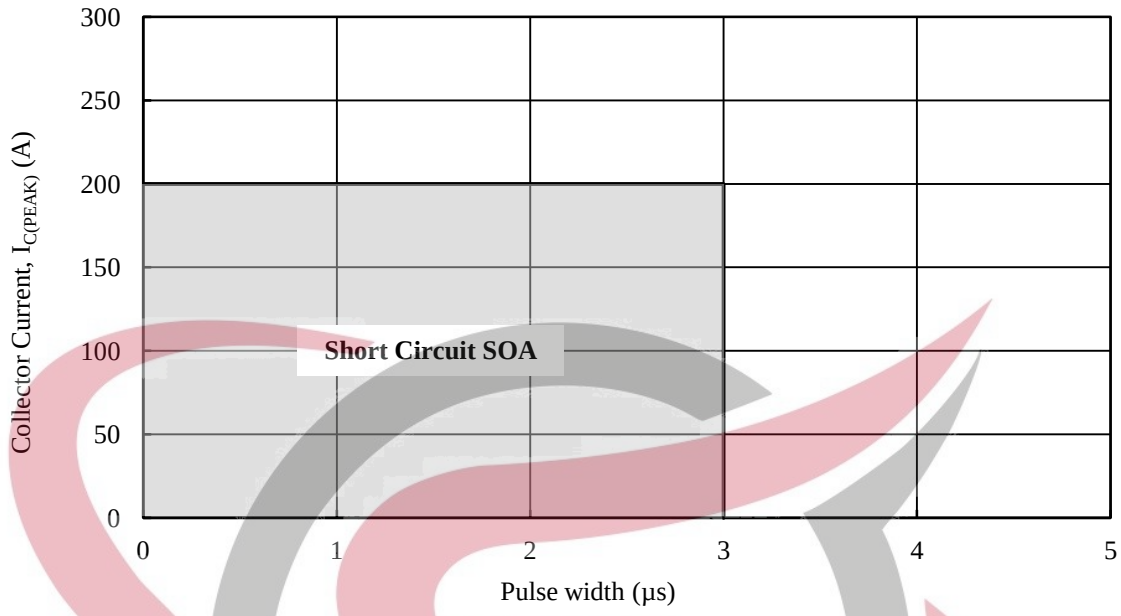
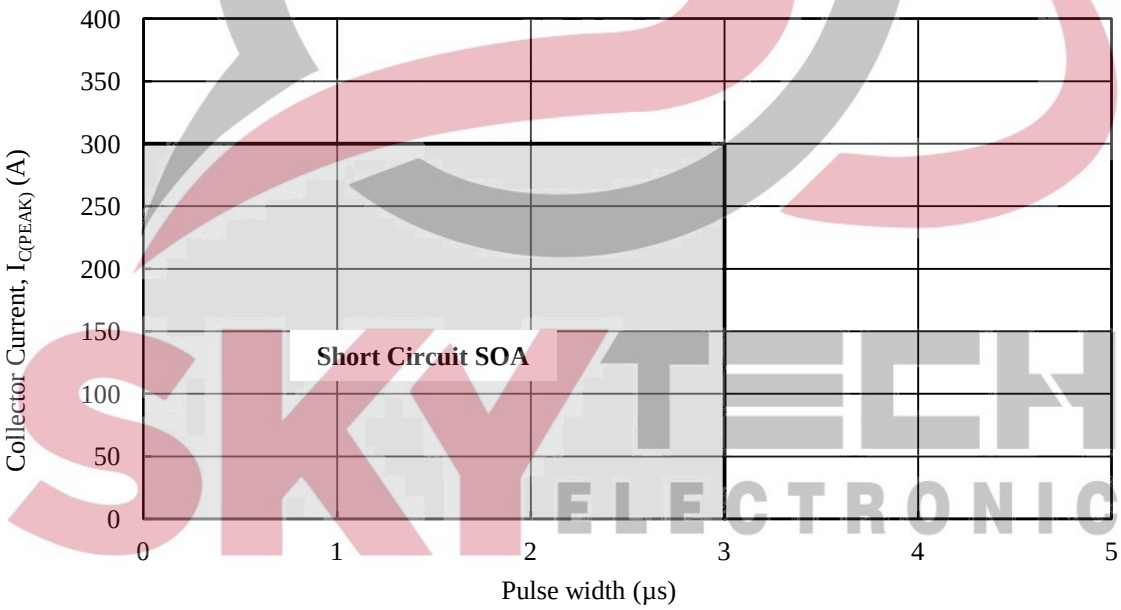
15.5.3. SCM1265MF, SCM1245MF



15.5.4. SCM1256MF, SCM1246MF



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16. Pattern Layout Example

The following show the schematic diagrams of a PCB pattern layout example using an SCM1200MF series device. For our recommended terminal hole size, see Section 10.4.

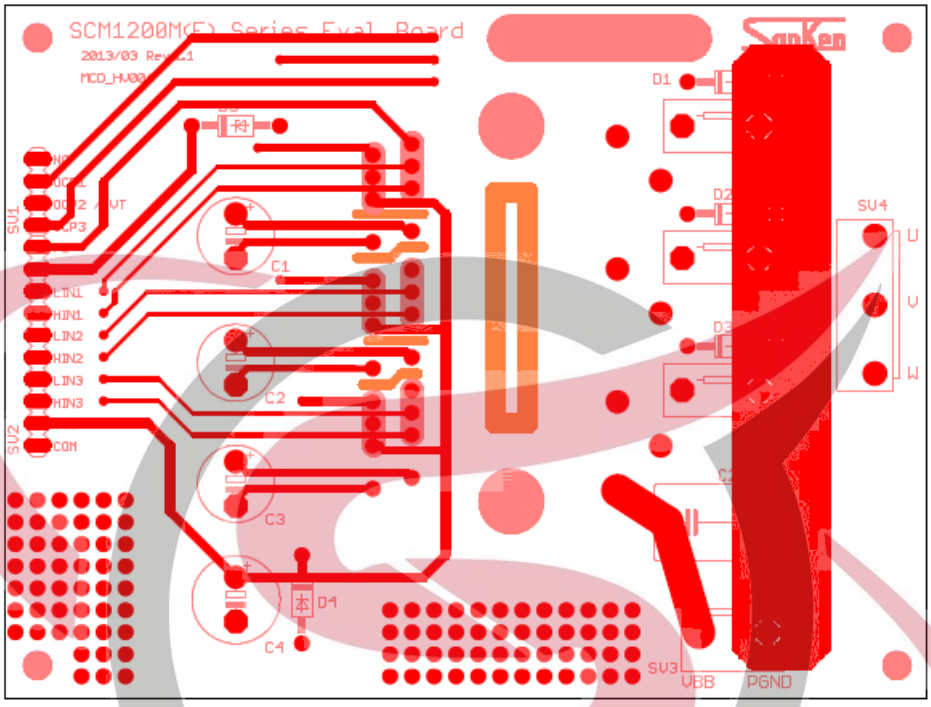

Figure 16-1. Top view

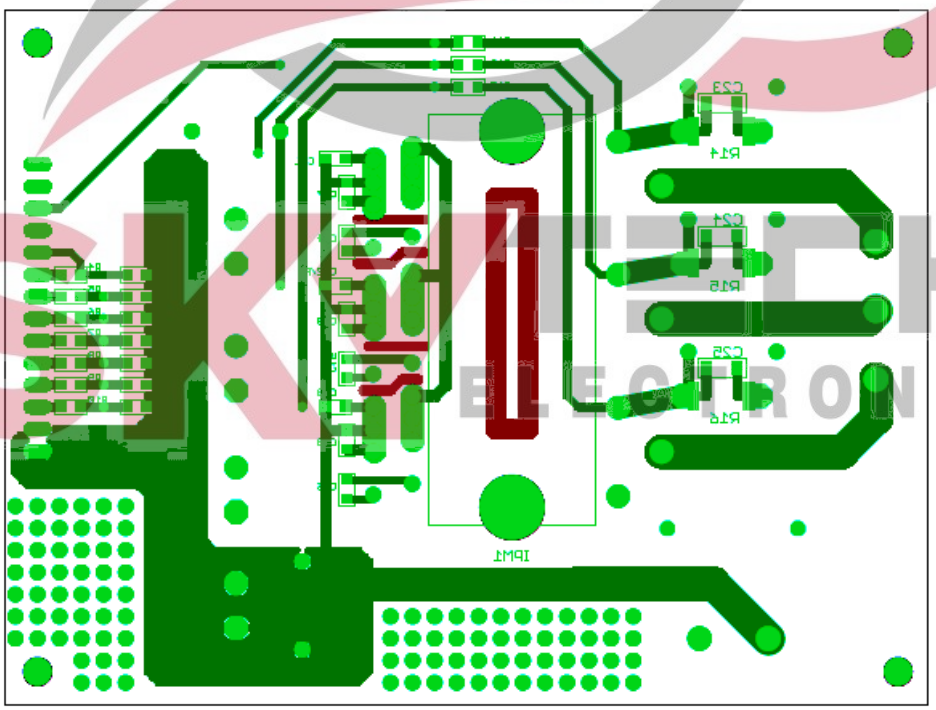

Figure 16-2. Bottom view

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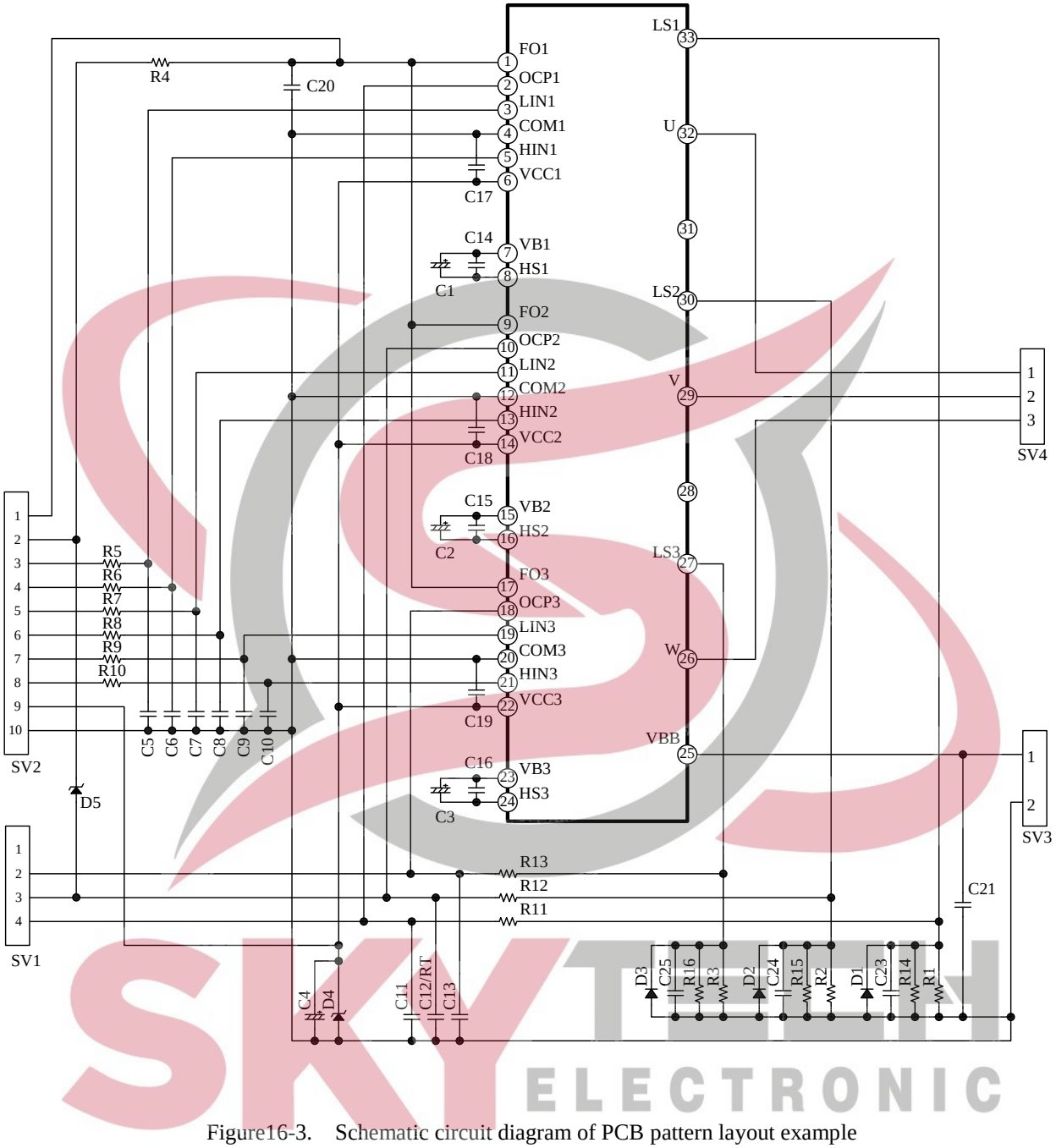

Figure16-3. Schematic circuit diagram of PCB pattern layout example

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17. Typical Motor Driver Application

This section contains information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- Motor driver specifications

IC	SCM1242MF
Main Supply Voltage, V_{DC}	300VDC (Typ.)
Output Power Rating	1.35 kW

- Circuit diagram

See Figure16-3.

- Bill of materials

Symbol	Part type	Ratings	Symbol	Part type	Ratings
C1	Electrolytic	47 µF, 50 V	R1*	Metal plate	27 mΩ, 2W
C2	Electrolytic	47 µF, 50 V	R2*	Metal plate	27 mΩ, 2W
C3	Electrolytic	47 µF, 50 V	R3*	Metal plate	27 mΩ, 2W
C4	Electrolytic	100 µF, 50 V	R4	General	4.7 kΩ, 1/8W
C5	Ceramic	100 pF, 50 V	R5	General	100 Ω, 1/8W
C6	Ceramic	100 pF, 50 V	R6	General	100 Ω, 1/8W
C7	Ceramic	100 pF, 50 V	R7	General	100 Ω, 1/8W
C8	Ceramic	100 pF, 50 V	R8	General	100 Ω, 1/8W
C9	Ceramic	100 pF, 50 V	R9	General	100 Ω, 1/8W
C10	Ceramic	100 pF, 50 V	R10	General	100 Ω, 1/8W
C11	Ceramic	0.01 µF, 50 V	R11	General	100 Ω, 1/8W
C12/RT	Ceramic	0.01 µF, 50 V	R12	General	100 Ω, 1/8W
C13	Ceramic	0.01 µF, 50 V	R13	General	100 Ω, 1/8W
C14	Ceramic	0.1 µF, 50 V	R14*	General	Open
C15	Ceramic	0.1 µF, 50 V	R15*	General	Open
C16	Ceramic	0.1 µF, 50 V	R16*	General	Open
C17	Ceramic	0.1 µF, 50 V	D1	General	1 A, 50 V
C18	Ceramic	0.1 µF, 50 V	D2	General	1 A, 50 V
C19	Ceramic	0.1 µF, 50 V	D3	General	1 A, 50 V
C20	Ceramic	0.01 µF, 50 V	D4	Zener	V_Z = 20 V, 0.5 W
C21	Film	0.1 µF, 630 V	D5	General	Open
C22*	Ceramic	0.1 µF, 50 V	SV1	Pin header	Equiv. to MA04-1
C23*	Ceramic	0.1 µF, 50 V	SV2	Pin header	Equiv. to MA10-1
C24*	Ceramic	0.1 µF, 50 V	SV3	Connector	Equiv. to B2P3-VH
C25	Ceramic	Open	SV4	Connector	Equiv. to B3P5-VH
			IPM1	IC	SCM1242MF

* Refers to a part that requires adjustment based on operation performance in an actual application.

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